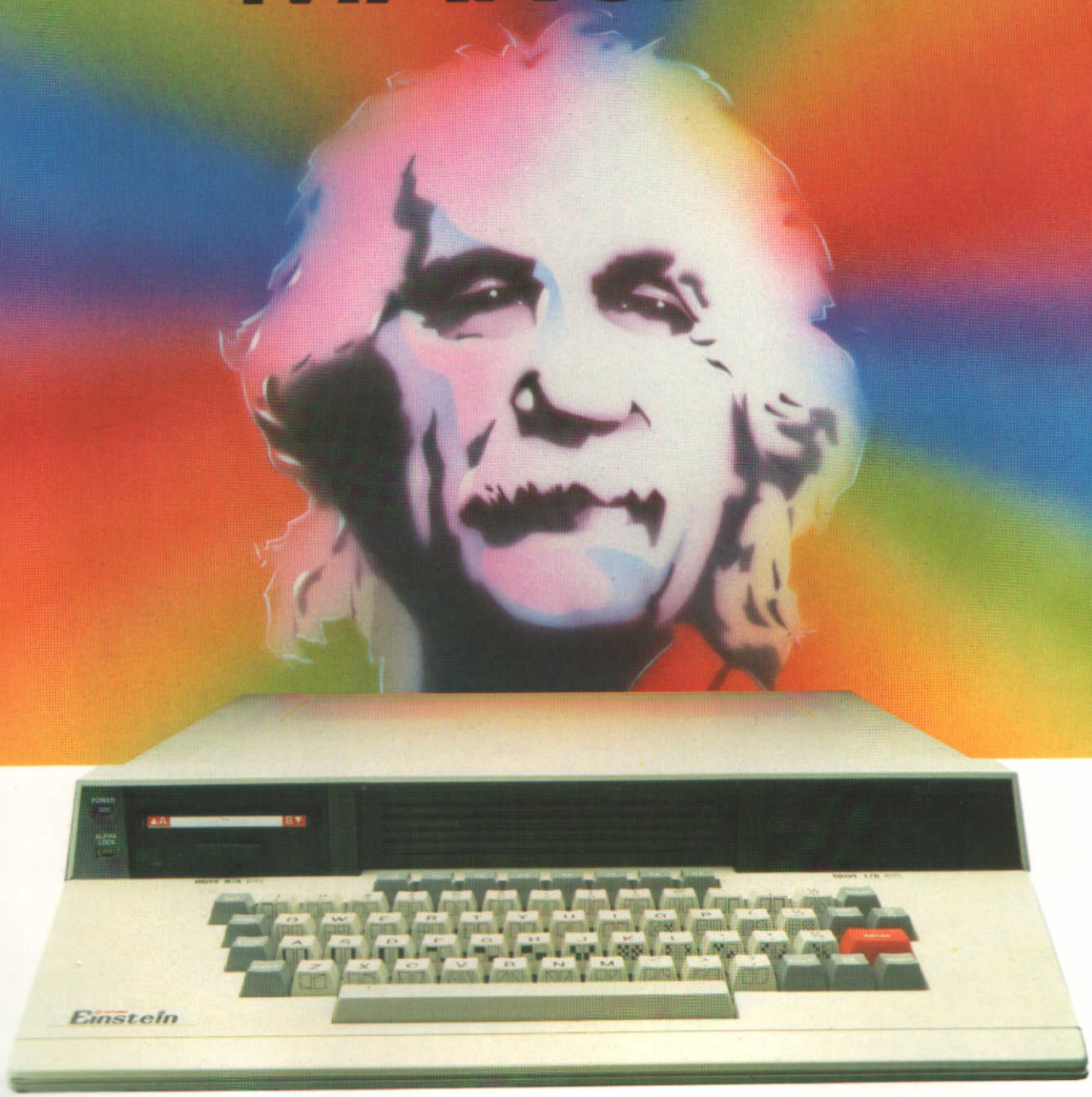
HARDWARE MANUAL



TATUNG

Einstein

COLOUR MICRO COMPUTER

1. GENERAL DESCRIPTION & SPECIFICATION

1.1 GENERAL

The EINSTEIN Home Computer - Model TC01, features modular construction for easy service access and incorporates its own internally mounted, fully screened switch-mode power supply.

As standard, the computer is supplied with one integrally mounted disc-drive unit for use with 3" floppy-discs.
Provision is made within the computer housing and fascia panel, for the installation of a second disc-drive unit, should this be required. (See Appendix B).

Facilities are available for feeding the display monitor with either YUV or, with RGB signal outputs which are selectable by means of simple internal link adjustments. (See Appendix A).

Provision of a comprehensive array of 'user' input/output ports and connector sockets allows the use of a wide variety of peripherals for expansion of the system. (see Appendix B)

1.2 HARDWARE SPECIFICATION - GENERAL

The general Hardware Specification for the Einstein Home Computer - Model TC01 is given following.

Please Note: The manufacturers retain the right to change, alter or modify, parts, components or specifications as deemed necessary in order to maintain or improve product performance, quality assurance, and/or specifications.

Consequently, this manual may be subject to change from time-to-time and no responsibility for errors or omissions as a result of change can be accepted.

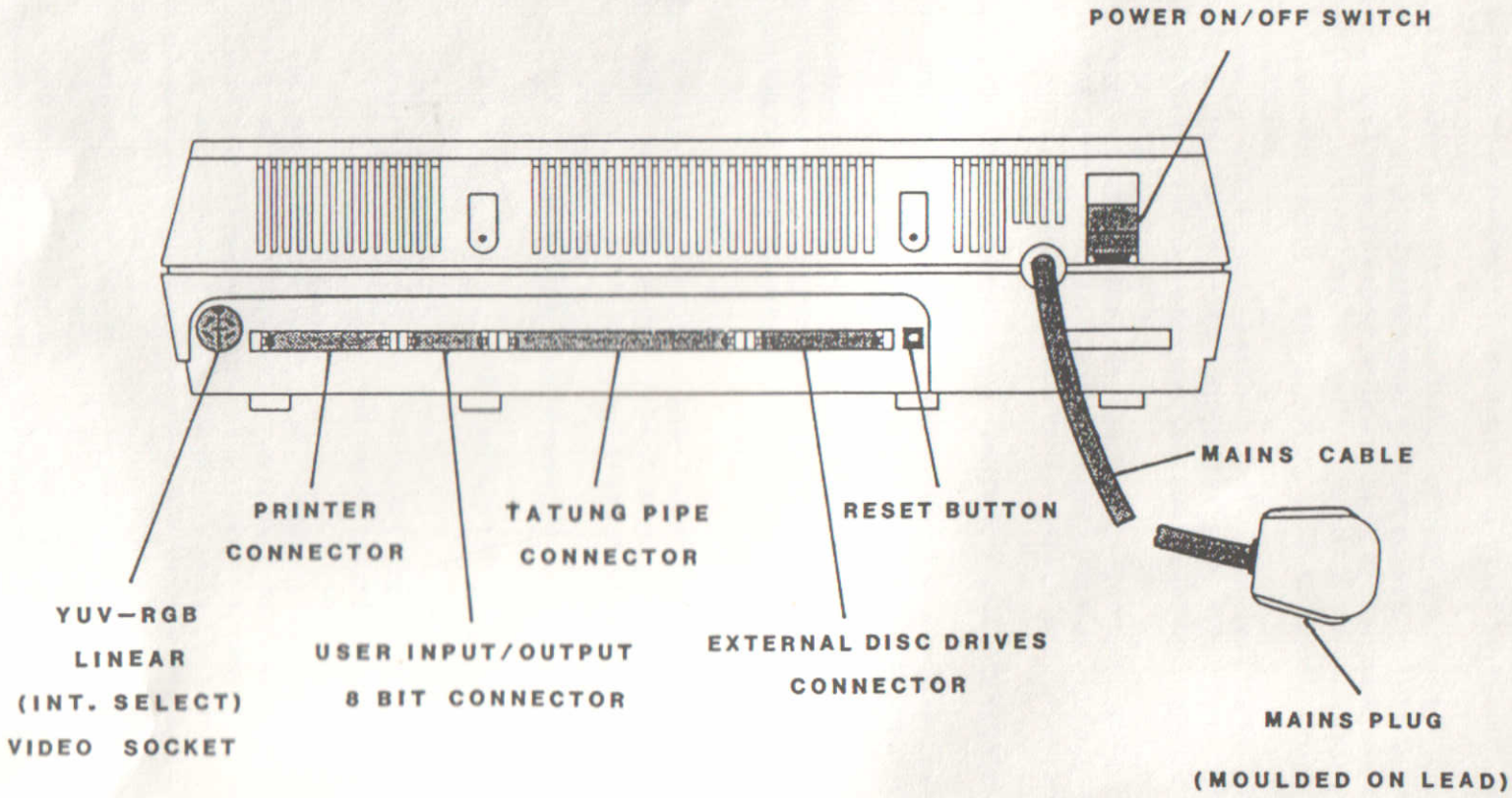
1.2.1 EINSTEIN Home Computer - Hardware Specification

CPU — Z80-clock frequency 4MHz.

MEMORY — 64k RAM
8k ROM with expansion for up to 32k internally.
16k separate video RAM.

DISPLAY — Hi-res. graphics 256 x 192 pixels, plus 32 planes of "sprites". In addition to "Sprites" there is a text/graphics and backdrop plane.
The display is capable of 16 colours:—

Transparent	Dark Blue	Mid Red	Dark Green
Black	Pale Blue	Pale Red	Magenta
Mid Green	Light Yellow	Dark Red	Grey
Pale Green	Cyan	Dark Yellow	White



VIEW FROM BACK OF COMPUTER

RS232-C Port:	Full duplex capability to RS 232-C/V24 standards. Transmission speeds are software programmable between 75 and 9600 bauds.
Signals Available:	Tx data, Rx data, RTS, CTS, Ground.
User Port:	8 bit bi-directional, with strobe and ready signals - TTL levels.
Analogue to Digital Converter:	4 channels, 8 bits resolution. Conversion speed less than 40us. Input range 2V.
Printer Output:	Centronics interface standard.
Tatung 'Pipe':	Z80A buffered bus to TTL levels, with clock, and control signals.
External Disc:	Provides signals for up to two self-powered external disc drives. Either 3 inch Compact Floppy 3 ½" micro floppy disc, or 5 ¼" mini floppy disc.

SOUND GENERATOR

A means of providing a variety of sounds, including chromatic music, with envelope shaping is provided. The sound generator has three "voices".

Sound Output: 250mW into internal 3 ½" x 2 ¼" Elliptical loudspeaker.

KEYBOARD

Full travel typewriter style QWERTY keyboard.

1. 48 alphanumeric/graphics keys, 8 function keys and 11 'control' keys.
2. All keys to have n lockout with 1 key roll-over.
3. Automatic repeat.
4. Programmable repeat delay and repeat speed.

DISC DRIVES	Teac FD30A	3 inch disc drive is incorporated.
	Specification:	Single sided 100 tpi 40 tracks MFM coding Disc fully enclosed in a cassette.
	Access Time:	12ms track-track 171ms average
	Transfer rate	250k bit/sec.
	Sectors/Track	10
	Bytes/Sector	512
Media Specification		500k byte unformatted capacity (250k/side) 400k byte formatted (200k/side) 80 tracks (40/side) Double density (MFM) recording 100 tpi Double sided 'flip-over' cassette.

2. GENERAL SERVICING NOTES

2 1. GENERAL PRECAUTIONS

To prevent damage and ensure correct functioning of the microcomputer, it is recommended that no form of repair, maintenance, or service, be attempted by any person other than a competent engineer.

2.1.1 Safety and Isolation - Power Supply

The microcomputer switched mode power supply incorporates a printed circuit panel, sections of which are always live regardless of the mains supply polarity. Therefore in the interests of safety, whenever servicing operations are being carried out, the power supply should be supplied through a mains isolation transformer of at least 200 watts rating.

2.1.2 Approved Components

Components marked ⚠ on the parts list and circuit diagram are safety approved types and should be replaced only with components supplied or approved by our Service Department. It is also recommended that components not marked with the safety symbol should be replaced by parts of the type originally fitted, and this applies particularly to those resistors which are stood off the printed wiring board.

2.1.3 Handling Precautions - Static Electrical Charges.

The microcomputer contains devices which may be damaged by static electrical charges during handling. These devices are indicated by a ⊗ symbol on the circuit diagrams. When replacing, or handling these devices, care should be taken. Soldering irons should be earthed, and personnel should use wrist straps earthed via a 1M resistor. If the later is not practicable, they should discharge themselves of any static electricity, by touching an earthed point.

Static sensitive devices should be packed in suitable conductive containers.

2.1.4 Component Replacement

Before removing or replacing any parts or components, in particular static sensitive devices, always disconnect the microcomputer from the mains supply.

The other precautions listed previously should also be observed when servicing this equipment.

2.2 CONSTRUCTION AND SERVICE ACCESS

2.2.1 General

The EINSTEIN microcomputer features modular construction which allows easy access for service, or for the installation of a second disc drive, should this be required.

To gain accesss - refer to the notes following:-

NOTE: Before commencing - first switch-off the power supply, unplug the mains lead from the mains supply and disconnect all other external inter-connecting cables.

2.2.2 Cover

Removal: The moulded cover on top of the microcomputer may be removed as follows:-

1) Unscrew and remove the 2 retaining screws located in the rear face of the cover.

2) Slide the cover towards the rear of the unit - and in the same movement - lift the back of the cover gently, to disengage and clear from their respective locations in the base unit assembly, the 4 retaining lugs moulded into the cover's front top and sides.

3) Lift the cover away to provide access to the microcomputer's interior.

Re-assembly: When re-assembling the cover:-

1) Ensure the 4 retaining lugs are correctly located into their respective slots and into the retaining lip on the moulded base unit assembly.

2) Finally, check that the cover and base are correctly aligned along their edges, then press the cover down evenly onto the base moulding and refit the 2 retaining screws.

2.3. SUB-ASSEMBLIES

The microcomputer in standard form comprises the following sub-assemblies:-

MAIN PRINTED CIRCUIT BOARD ASSEMBLY
KEYBOARD ASSEMBLY
SWITCHED-MODE POWER SUPPLY UNIT
DISC DRIVE UNIT

These sub-assemblies, together with interconnection details of the internal wiring, routing, colour coding and functions, are shown in completed assembly form in Drawing 'TC01 INTERCONNECTION/LAYOUT DIAGRAM - Drawing No. 85-4645-2 and drawing 'CONNECTION & CIRCUIT DIAGRAM FOR LOUDSPEAKER, LED BOARD & KEYBOARD' in this section following.

If required - a second disc drive unit may be installed - provision is made for this in the main base unit assembly. (See APPENDIX B)

Sub-assembly Access
Access to the various sub-assembles comprising the microcomputer may be achieved in the manner described following:-

2.3.1 Main Printed Circuit Board Assembly

The main printed circuit board assembly may be removed from the base unit assembly using the following sequence.

NOTE: If a second Disc Drive unit is fitted (Drive 1/B ⎓) it will be first necessary to remove the second disc drive before the Main Printed Circuit Board Assembly can be removed as detailed following. (See Section 2.3.3 on Disc Drive Unit)

To remove the PCB assembly:-

1) Unplug multiway connectors - M006 - Keyboard
" " " " " - M011 - Speaker
" " " " " - M008 - Disc Drive
" " " " " - M007 - Switched Mode Power Supply
" " " " " - M005 - Internal Disc Drive
" " " " " - M012 - Signal Lead LED assembly

2) Detach the push-on knob from the volume control located at the side of the unit.

3) Remove the power supply unit as detailed (See Section on Switch Mode Power Supply, Section 2.3.4)

4) Unscrew the 9 screws retaining the main PCB to the base unit. These are located around the edge of the PCB. The board assembly may then be withdrawn from the base unit by first sliding the board forward to clear the rear connections, then moving the board sideways and lifting to clear the disc drive brackets.
Re-assemble in the reverse order.

2.3.2 Disc Drive Unit

The Disc Drive Unit(s), is housed in a metal support bracket attached to the floor of the base unit moulding. 4 screws are used to mount each Disc Drive unit.

It is not necessary to remove this bracket in order to detach the Disc Drive unit from the main assembly. It may be necessary however, to detach the speaker unit - in order to provide unrestricted access to the disc drive mounting screws.

To remove the Disc Drive Unit(s):-

1) Supporting the front of fascia - remove the 2 screws securing the speaker unit to the speaker baffle moulding. Unplug speaker connector M011 from Main PCB and detach speaker unit.

2) Unplug multiway connector - M005 - (Internal Single Disc Drive Control Harness Lead Set)
" " " " " - M008 - Disc Drive power lead (0/A)
Unplug multiway connector - M009 - Disc Drive power lead (1/B) (if 2nd unit is fitted)
" " " " - M005 - Internal Dual Disc Drive Control Harness lead set (if 2nd unit is fitted)

3) Slacken-off only - but do not remove - 2 screws on each side (4 total) of each disc drive unit.

4) Remove the disc drive by sliding the unit back and lifting upwards to clear the retaining slots in the support brackets.

Re-assembly:
Re-assemble in reverse order - then retighten all retaining screws - **DO NOT OVERTIGHTEN.**

2.3.3 Keyboard Assembly

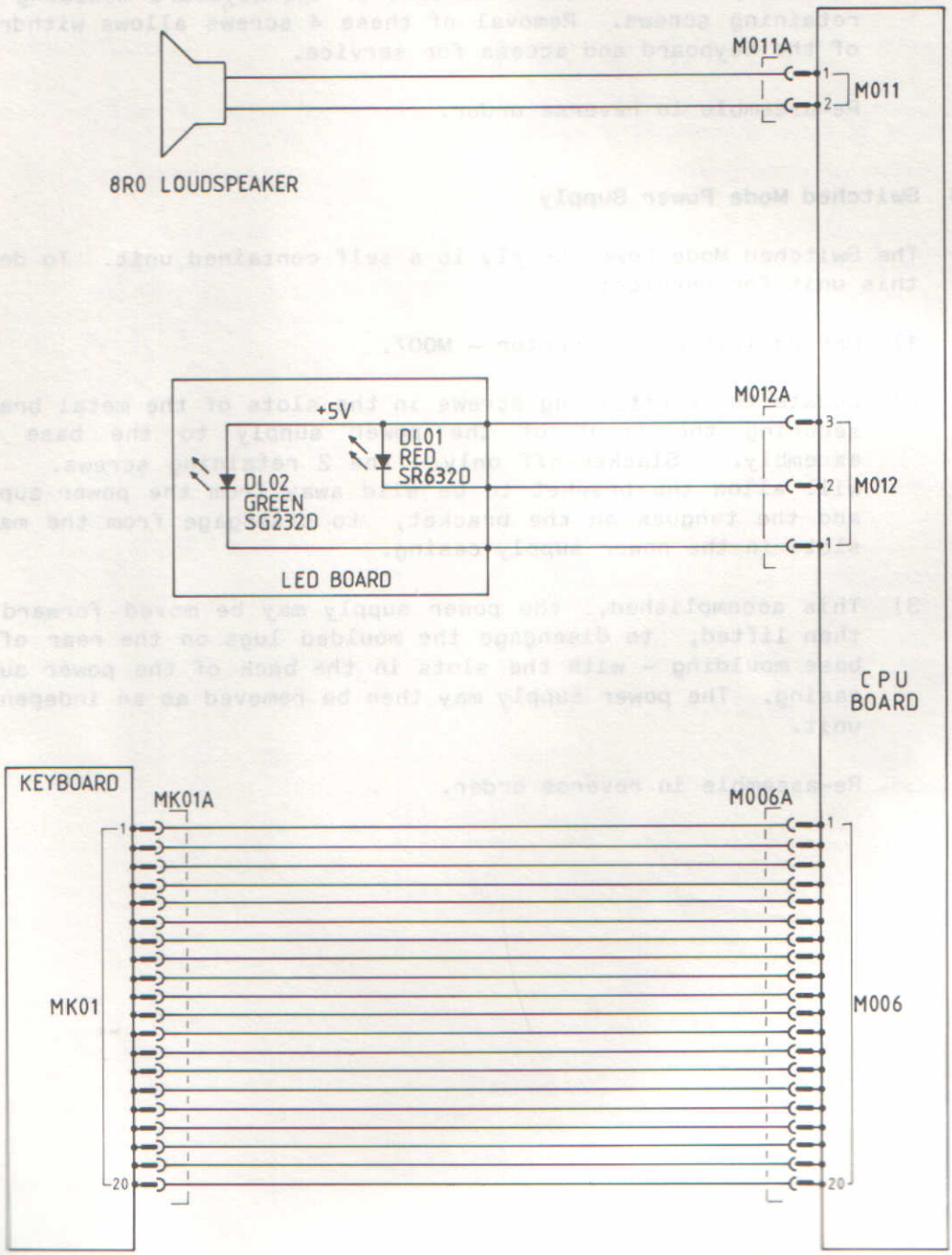
To access the Keyboard assembly - proceed as follows:-

1) Remove Disc Drive(s) as detailed previously above.

2) Unplug Multiway connectors - M006 - Keyboard
" " " " " - M011 - Speaker
" " " " " - M012 - LED. assembly

3) From front **underside** of base unit - remove 3 recessed screws holding front of keyboard moulding to base unit.

4) From inside of base unit - slacken-off only - 4 retaining screws on L/H and R/H sides, (2 each side) - holding speaker moulding slotted angled brackets to Disc Drive metal brackets. Slacken-off also - 2 retaining screws (1 each side), holding the slotted angled brackets on the speaker moulding, to the 2 moulded pillars on the base unit.



CONNECTION AND CIRCUIT DIAGRAM
FOR LOUDSPEAKER, LED BOARD AND KEYBOARD
DRAWING No 85-4664-9

5) The Keyboard/Speaker assembly may then be withdrawn as a complete unit from the base unit assembly.

6) The Keyboard PCB complete with keyswitches, is fixed to four moulded pillars on the underside of the keyboard moulding by 4 retaining screws. Removal of these 4 screws allows withdrawal of the keyboard and access for service.

Re-assemble in reverse order.

2.3.4 Switched Mode Power Supply

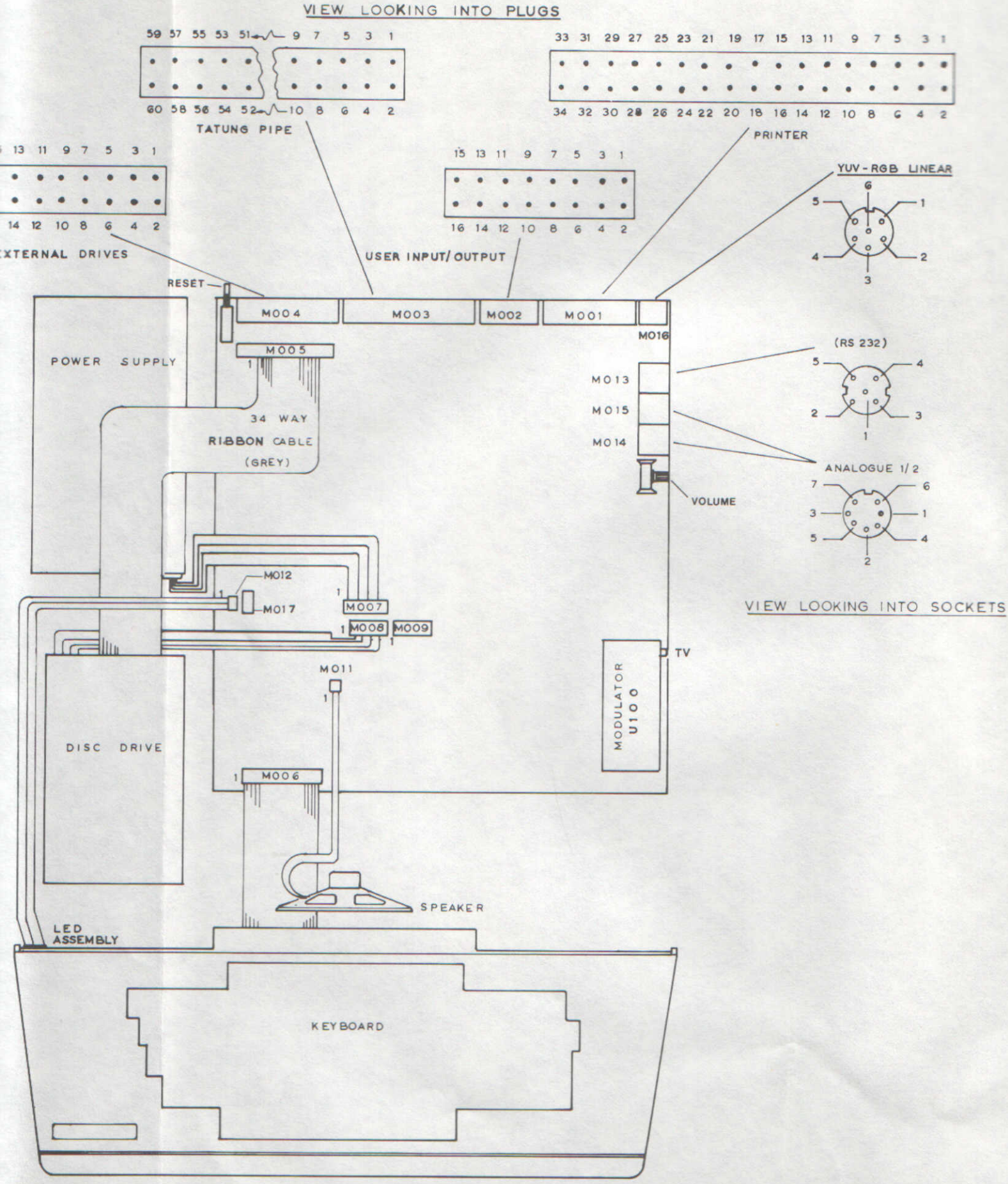
The Switched Mode Power Supply is a self contained unit. To detach this unit for service:-

1) Unplug multiway corrector - M007.

2) Locate the 2 retaining screws in the slots of the metal bracket securing the front of the power supply to the base unit assembly. Slacken-off only - the 2 retaining screws. This will allow the bracket to be slid away from the power supply, and the tongues on the bracket, to disengage from the mating slots in the power supply casing.

3) This accomplished, the power supply may be moved forward and then lifted, to disengage the moulded lugs on the rear of the base moulding - with the slots in the back of the power supply casing. The power supply may then be removed as an independent unit.

Re-assemble in reverse order.



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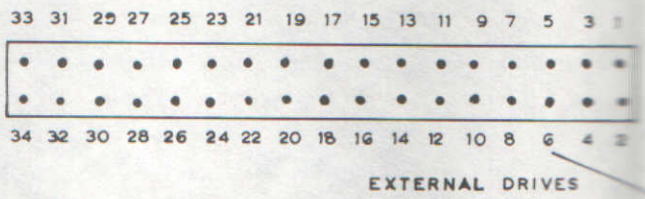


DISC DRIVE M005

PIN	FUNCTION
1	0V
2	RESERVED
3	0V
4	RESERVED
5	0V
6	DS3
7	0V
8	INDEX
9	0V
10	DS0
11	0V
12	DS1
13	0V
14	DS2
15	0V
16	MON
17	0V
18	DIR
19	0V
20	STEP
21	0V
22	W/DATA
23	0V
24	W/GATE
25	0V
26	TR00
27	0V
28	WP
29	0V
30	RD
31	0V
32	SS
33	0V
34	RESERVED

DISC 0 POWER M008

PIN	FUNCTION	COLOUR
1	12V	white / red
2	0V	white / black
3	0V	white / black
4	5V	white/orange

DISC 1 POWER M009

PIN	FUNCTION	COLOUR
1	12V	white / red
2	0V	white / black
3	0V	white / black
4	5V	white/orange

POWER M007

PIN	FUNCTION	COLOUR
1	12V	white / red
2	0V	white / black
3	N/C	
4	5V	white/orange
5	-12V	white / pink

KEYBOARD M006

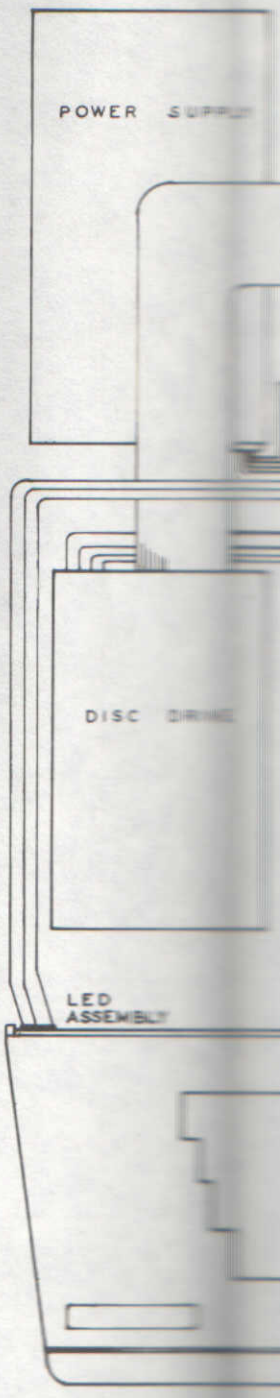
PIN	FUNCTION
1	A0
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	B0
10	B1
11	B2
12	B3
13	B4
14	B5
15	B6
16	B7
17	SHIFT
18	CTRL
19	0V

SPEAKER M011

PIN	FUNCTION	COLOUR
1	0V	white
2	SIG.	white

LED ASSY. M012

PIN	FUNCTION	COLOUR
1	POWER ON	white/yellow
2	ALPH LOCK	white/violet
3	5V	white/orange



T001 - INTERCONNECTION/LAYOUT DIAGRAM

3. MICRO COMPUTER

3.1 GENERAL

The computer uses the Z80A microprocessor operating at a 4MHz clock-rate. There are several blocks of memory including 16k bytes of video RAM which is accessed via the Video Display Processor and up to 32k bytes of EPROM/ROM which is "paged" into the bottom half of the 64k byte CPU memory (RAM) area. There are also a number of LSI devices which are attached to the processor bus to provide peripheral functions.

Because devices from a variety of manufacturers and microprocessor familes are used in the computer, some extra logic has been necessary to interface these parts to the Z80A bus architecture. In particular it has been necessary to generate interrupt vectors for non-Z80A parts to allow the correct Z80 interrupt structure to be implemented.

3.1.1 Circuit Diagrams

In the circuit description following, reference should be made to the main circuit diagram of the 'EINSTEIN TC01 HOME COMPUTER' - Drawing No. 85-4584-7 and to the 'FUNCTIONAL BLOCK DIAGRAM' in Fig.3.2. The physical location on the main printed circuit board assembly of each functional circuit block described, is shown in Fig.3.3 'PCB FUNCTIONAL BLOCK LAYOUT' diagram.

Where necessary, descriptions of individual circuit blocks are supplemented by additional diagrams as an aid to the descriptions.

3.2. CIRCUIT DESCRIPTIONS

Each functional circuit block is described in detail separately below. No attempt will be made to describe the internal architecture of any device, except where this pertains to the external circuitry used, reference to the appropriate device data should be made for this information.

3.2.1 Central Processor Unit (CPU)

System Clock Generation

The CPU runs at a clock-rate of 4MHz, this clock-signal is provided by an 8MHz master clock formed by I047a, I047b, RO32, RO33, C010, X002. The signal is then partially buffered by I047c before being fed to a 4-stage binary counter, I048, to be divided to give 4MHz and 2MHz clocks to run the processor and most of the peripheral i.c.'s.

The 4MHz clock is buffered by a TTL inverter and discrete active pull-up circuit comprising I047d Q004, R034, R035, R036, C011. This ensures that the clock rise and fall times meet the specific requirements of the Z80A devices, i.e. rise and fall-times are <30ns. (See Fig.3.1 - 'SYSTEM CLOCK TIMING').

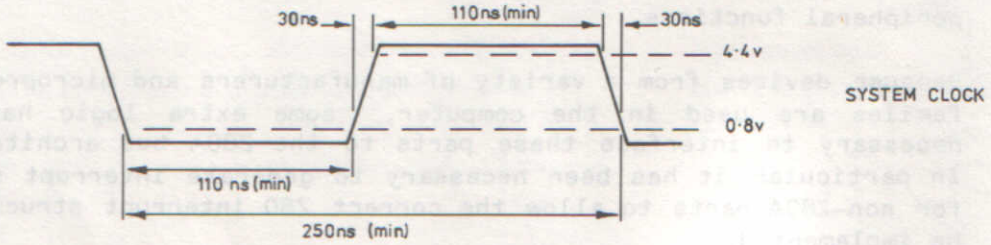


Fig.3.1 SYSTEM CLOCK TIMING

CPU Control Signals

Reset pulses for the system are provided by a monostable multivibrator, I035a, which provides a single >50us pulse from its complementary outputs when triggered at power-up, or via reset-switch S001. On power-up capacitor C025 is charged via R055 such that the input (pin 4) of I052b reaches a logic '1' approximately 575ms after power-up. The relative values of C020 and C025 ensure that pin 5 I052b is still at logic '1' at this point, the output (pin 6) of I052b therefore changes state to logic '0' triggering the monostable I053a. The reset switch (S001) discharges C020 via R053 this causes the inputs (pins 1 & 2) of I052a to change state from logic '0' to logic '1', this in turn causes the output (pin 6) of I052b to change state from logic '1' to logic '0'. This triggers the monostable (pin 1) I053a which gives a single pulse of 50us, the pulse-width being set by R056, C026. Reset signals of both polarities are provided at pins 4 and 13 of I053a to match the peripheral i.c.'s used.

The Non-maskable Interrupt ($\overline{NMI}$) pin 17, Interrupt ($\overline{INT}$) pin 16, Wait ($\overline{WAIT}$) pin 24, and Bus Request (BUSREQ) pin 25 are pulled to a logic '1' by resistors R001, R002, R003 and R004.

The CPU address-bus signals are buffered by two octal tri-state buffers I002 and I003 before being fed to the address-bus proper. The CPU data-bus is buffered by an octal bus transceiver I004, the direction of data transfer is set by I022d which allows input from the data-bus to the CPU during a Read ($\overline{RD}$) or Interrupt-Acknowledge (INA) cycle. The CPU control-bus outputs only are buffered by an octal tri-state buffer I005. The Bus-Acknowledge signal ($\overline{BUSACK}$) from the CPU is used to put I002, I003, I004, and I005 into

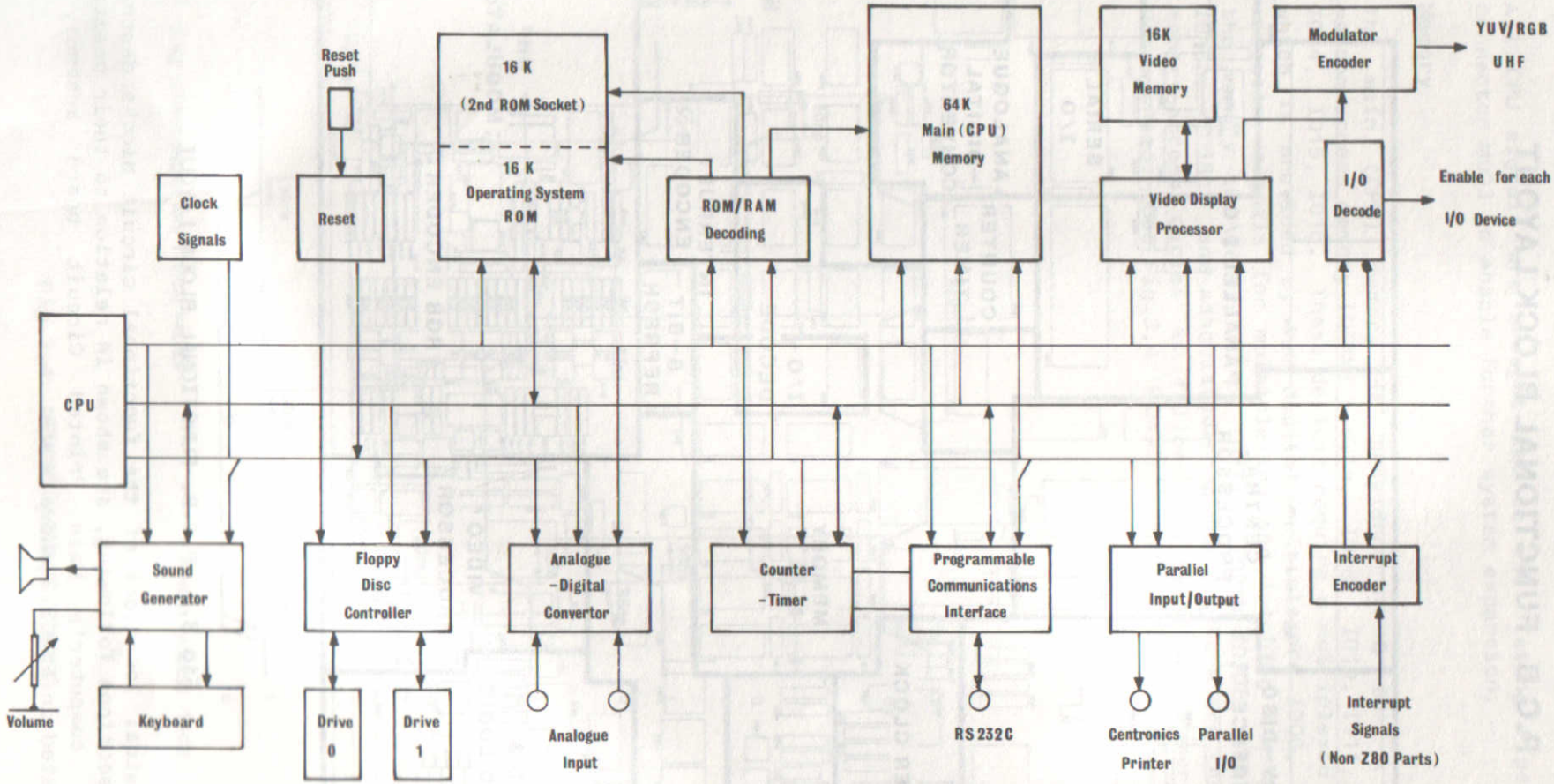


Fig. 3.2 FUNCTIONAL BLOCK DIAGRAM

P.C.B. FUNCTIONAL BLOCK LAYOUT

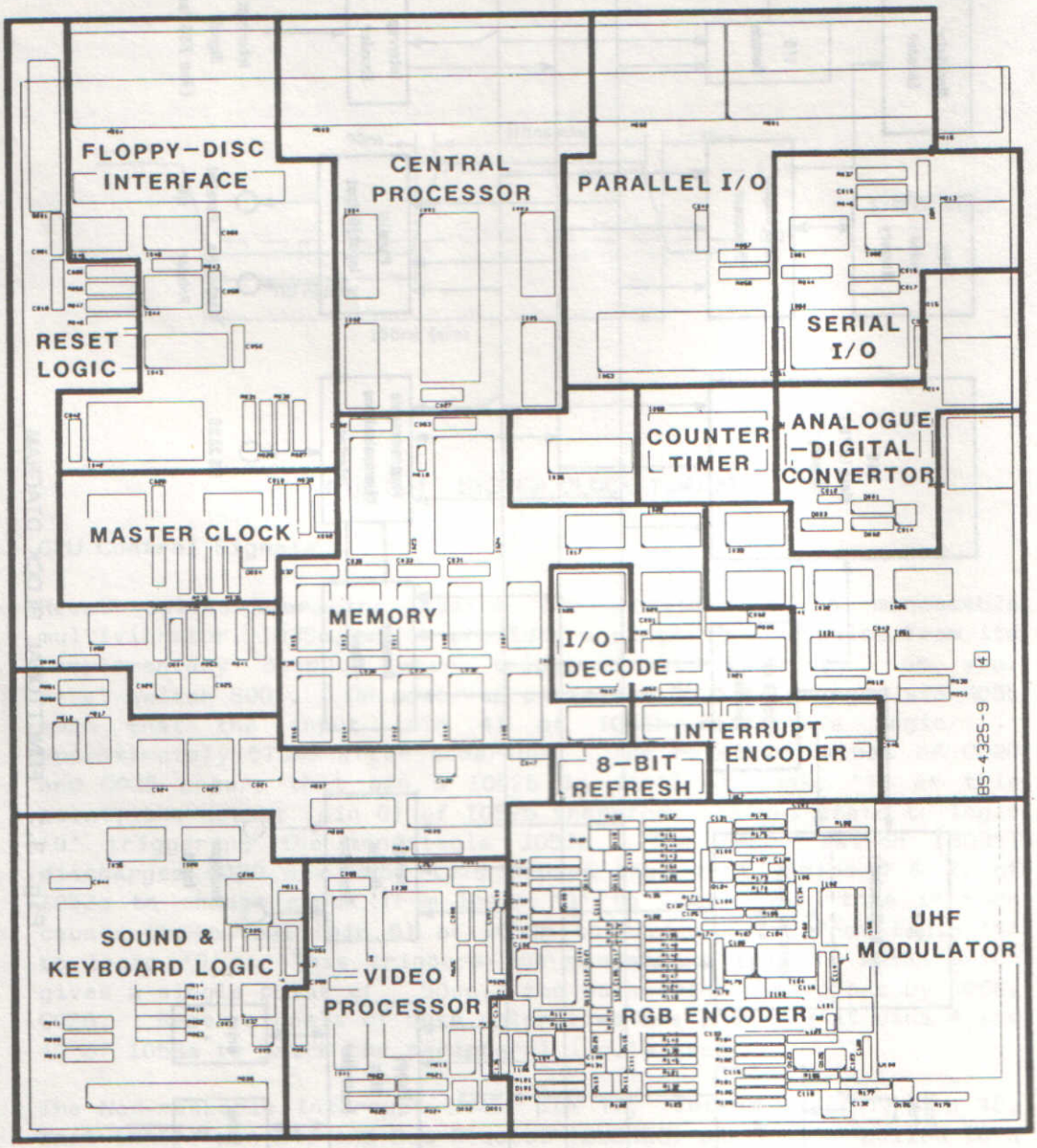


Fig 3.3 P.C.B. FUNCTIONAL BLOCK LAYOUT

The physical locations of the functional circuit blocks described in the sections following, are shown in relation to their positions on the computer's Main Printed Circuit board assembly as illustrated in Fig.3.3 above.

tri-state mode via I022b whenever the CPU relinquishes control of the system buses on detecting a logic '0' on the $\overline{\text{BUSREQ}}$ line.

All CPU signals are brought out to the "Tatung Pipe" expansion connector M003 to enable further system expansion.

3.2.2 Memory

The main (CPU) memory is provided by 8 64k x 1 dynamic random-access memory (DRAM) i.c.'s, I008, I010, I011, I012, I013, I014, I015, I016. These devices require a multiplexed address-bus which is provided by two digital multiplexors I006, I007. The necessary signals for multiplexing and latching the address into the memory are generated by I017a, I021b I020b, I018a, I020c, I018b, I018c, and associated components. There are three possible memory-access cycles as follows:- Refresh, Memory-Write and Memory-Read. (See Fig.3.4 'MEMORY ACCESS TIMINGS').

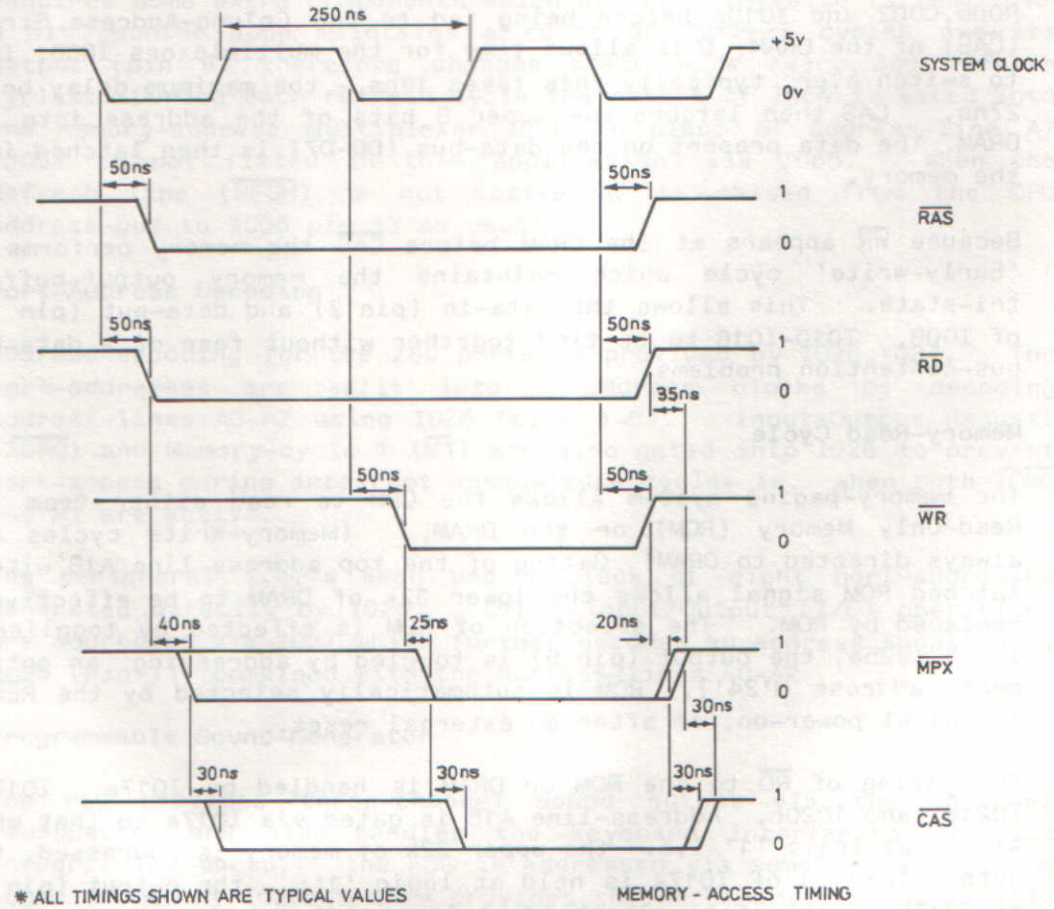


Fig.3.4 MEMORY ACCESS TIMING

Refresh Cycle

Only $\overline{MREQ}$ and the lower 7-bits of the CPU address-bus are active. Therefore I020b output (pin 6) is held at logic '1' and I018a (pin 3) is also held at logic '1'. Consequently I020c output (pin 8) is held at logic '1' and the lower 8 bits are switched onto the multiplexed address-bus (MA0-MA7). The Row-Address Strobe ($\overline{RAS}$) is then taken to logic '0' to latch the row address into memory in order to refresh that row of memory cells.

Memory-Write Cycle

During a memory-write cycle I020b output (pin 6) is held at logic '1' since $\overline{RD}$ (I020b,pin 5) is not active. The output (pin 8) of I020c is therefore at logic '1' which switches the lower 8 bits of the CPU address bus onto the multiplexed address-bus. These bits are then latched into the DRAM using the row-address strobe ($\overline{RAS}$). The $\overline{WR}$ signal becomes active, a minimum of 225ns, after $\overline{RAS}$ becomes active. This causes the output (pin 3) of I018a to change state to a logic '0' which consequently causes I020c output (pin 8) to also change state to logic '0' switching the upper 8 bits of the CPU address-bus onto the multiplexed address (MA0-MA7). The output (pin 8) of I020c is delayed via I018b, a resistor/capacitor network R006,C002 and I018c before being fed to the Column-Address Strobe ($\overline{CAS}$) of the DRAM, this allows time for the multiplexors I006, I007 to switch over, typically this takes 18ns - the maximum delay being 27ns. CAS then latches the upper 8 bits of the address into the DRAM. The data present on the data-bus (D0-D7) is then latched into the memory.

Because $\overline{WR}$ appears at the DRAM before $\overline{CAS}$ the memory performs an 'Early-Write' cycle which maintains the memory output-buffers tri-state. This allows the data-in (pin 2) and data-out (pin 14) of I008, I010-I016 to be tied together without fear of a data-bus bus-contention problems.

Memory-Read Cycle

The memory-paging system allows the CPU to read either from the Read-Only Memory (ROM) or the DRAM, (Memory-Write cycles are always directed to DRAM). Gating of the top address line A15 with a latched ROM signal allows the lower 32k of DRAM to be effectively replaced by ROM. The selection of ROM is effected by toggling a latch I025a, the output (pin 5) is toggled by addressing an output port (address H'24'). ROM is automatically selected by the $\overline{RESET}$ signal at power-on, or after an external reset.

The gating of $\overline{RD}$ to the ROM or DRAM is handled by I017a, I017b, I021b, and I020b. Address-line A15 is gated via I017a so that when A15 is at logic '1' i.e. the upper 32k of memory is addressed, the output (pin 3) of I017a is held at logic '1'; the output (pin 6) of I017b is therefore also held at logic '1' which prevents either ROM I023,I024 from being selected. In this case the signal from I017a (pin 3) is inverted and so I020b (pin 4) is held at logic '0'. When $\overline{RD}$ subsequently goes to its active, logic '0', state, I020b output (pin 6) will change state to logic '0' causing the

output (pin 3) of I018a also to change state to logic '0'. This then triggers the multiplex $\overline{MPX}$ and $\overline{CAS}$ signals as for a Memory-Write cycle.

When address-line A15 is at logic '0' the selection of ROM/DRAM is governed by the state of the latched $\overline{ROM}$ signal at the input (pin 2) of I017a. If ROM is selected i.e. I017a pin 2 is at logic '0' then I017a output (pin 3) will be also at logic '0', this signal is inverted by I021b and fed to I020b (pin 4) which gates out the $\overline{RD}$ signal to prevent $\overline{RD}$ from triggering a DRAM access. ROM-access is then initiated by gating the combined $\overline{MREQ}$ and $\overline{RD}$ signals from I017c (pin 8) to the inputs of I017d and I021a. I017d then selects I023 (pin 22) if A14 is also at logic '0' otherwise I024 (pin 22) is selected via I022a. Note that both ROM's have a further chip-enable (pin 20) which is fed directly from the latched ROM signal (I025a Pin 5), this ensures that both ROM devices are disabled into their stand-by (low-power consumption) mode when ROM-access is not required.

Eight-Bit Refresh Memory

Eight-bit refresh memory which may be fitted as I08, I010-I016 requires some extra components which are not otherwise fitted. An 8 bit counter I064 maintains a count of Refresh cycles and its output (pin 8) therefore changes state once every 256 refresh cycles. During each refresh cycle the output of I064 is gated into the memory-address multiplexor I006 in place of address-line A7 (J052 is not fitted in this application) via I065. When the Refresh line ($\overline{RFSH}$) is not active A7 is passed from the CPU address-bus to I006 pin 13 as usual.

3.2.3 Port-Address Decoding

Address-decoding for the Z80 ports is provided by I026,I027. The port-addresses are split into 8 address blocks by decoding address-lines A3-A7 using I026 (pins 1-5). Input-Output Request ($\overline{IORQ}$) and Memory-cycle 1 ($\overline{M1}$) are also gated into I026 to prevent port-access during interrupt-acknowledge cycles ie. when both $\overline{IORQ}$ and $\overline{M1}$ are active.

The peripheral i.c.'s each use a block of eight port-addresses generated directly by I026. Other Input/Output (I/O) operations are addressed via I027 which further decodes an address supplied by I026 (Pin 11) combined with the address-lines A0-A2

3.2.4 Programmable Sound-Generator

The PSG provides three-channel sound output via the internal loudspeaker and also handles the keyboard interfacing via two integral I/O ports. The PSG is addressed via some extra decoding logic formed by I028a,b this provides the necessary control signals for the PSG by combining $\overline{WR}$ and $\overline{PSG}$ to give a bus-direction signal (BDIR; I030 pin 27) and address-line A0 with $\overline{PSG}$ to give a bus-control signal (BC1; I030 pin 29). A "software-reset" is also

provided on two of the PSG-port addresses, this allows all of the PSG registers to be reset to a defined state via a port access. The "software-reset" is also fed to the Floppy-Disc controller (see section 3.2.6)

Keyboard Interface

The PSG I/O ports are set up by the Machine Operating-System (MOS) software such that port A (I030 pins 14-21) is an output port and port B (I030 pins 6-13) is an input port. As the PSG port inputs have internal pull-up resistors of 13k ohms, the input lines (I030 pins 6-13) and the inputs of I035 (pins 1-6,11,12) are held at logic '1' and I035 output (pin 8) is held at logic '0'. The output-port lines (I030 pins 14-21) are set to logic '0' by the MOS such that when a key depression is made on the keyboard matrix one of the input lines of I030 (and I035) will be connected to a logic '0' (see fig.3.5) If the key is held down then the MOS will start to strobe the input line selected.

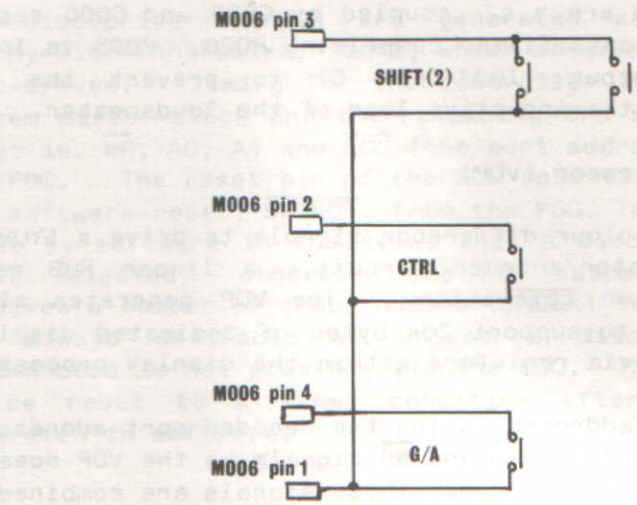
Keyboard Interrupt Logic

The four key-switches which do not use the keyboard matrix - 2 x SHIFT, CTRL, and GRAPH, are connected between the OV rail and pins 17-19 on the keyboard connector M006. These lines have pull-up resistors R008, R010, R011, and are connected to a tri-state buffer I036 which gates these signals onto the data-bus when the KYBDINTMSK port is read (from). If any key-switch is closed then the output (pin 8) of I035 changes state to logic '1' which gates the system clock (SYSCLK) into a latch I031a (pin 3) which sets the output (pin 5) to logic '0' to generate a keyboard interrupt.

If a reset (RESET) occurs or the Keyboard-Interrupt Mask (KYBDINTMSK) port is read (from) then I018a or I032d respectively preset I031a output (pin 5) to logic '1' to clear any keyboard interrupt. The latch I031b together with I032a form an interrupt-mask which is latched to either logic state by writing to data-bit 0 of the KYBDINTMSK port. If a logic '1' is written to this port or a RESET occurs then I031b output (pin 9) is preset to logic '1' i.e. keyboard interrupts are masked. The keyboard interrupt and interrupt mask signals are combined by I034a which gates the keyboard interrupt according to the state of the mask latch I031b and I047c inverts the resulting output which is fed into the interrupt-priority system - see section 3.2.8.

Audio Output

The audio frequency outputs from the PSG (I030 pins 4,3,38) are current sources terminated by resistors R013, R014, R015 respectively. The audio signals are then combined in the resistor network R018, R062, R063 and R016 and fed to R062, R063 and R016 and fed to an audio amplifier I037 together with its associated components. The resistor-capacitor combination R017, C004 form a



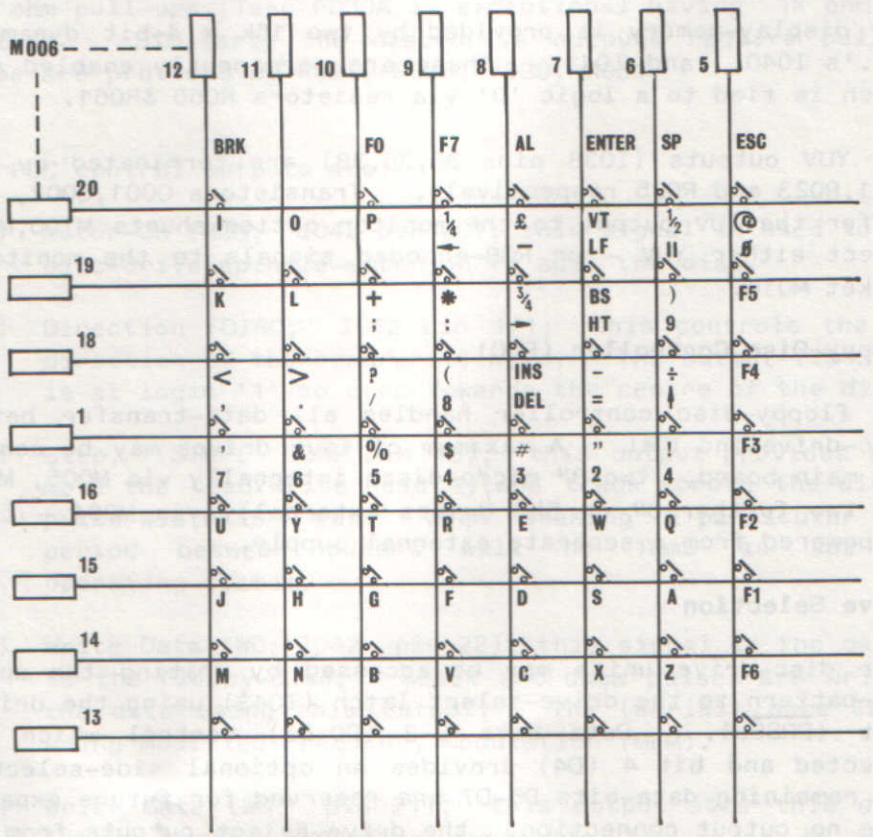


Fig. 3.5 KEYBOARD MATRIX

low-pass filter to reduce interference from the high-frequency digital signals present in the same area of the circuit. The input and output signals are a.c. coupled by C003 and C006 respectively and a further low-pass filter comprising R020, C005 is included at the amplifier output (I037 pin 5) to prevent the amplifier oscillating under the inductive load of the loudspeaker.

3.2.5 Video-Display Processor (VDP)

The VDP provides colour-difference signals to drive a (YUV) monitor or, via a modulator/encoder circuit, a linear RGB monitor or domestic UHF colour television. The VDP generates all of the necessary signals to support 16k bytes of dedicated display-memory which is accessed via registers within the display processor.

The VDP (I038) is addressed using the decoded port-address ($\overline{VDP}$) in conjunction with the Z80 $\overline{RD}$ and $\overline{WR}$ signals as the VDP does not have a "chip-select" input as such. These signals are combined by I032b and I032c to give chip-select Read ($\overline{CSR}$) and Chip-Select Write ($\overline{CSW}$) - pins 15 and 14 of I038 respectively.

All internal timing for I038 is derived from a 10.68-MHz crystal-oscillator which uses X001 as a reference together with C007, and C008.

The display-memory is provided by two 16k x 4-bit dynamic memory i.c.'s I040, and I041. These are permanently enabled via pin 7 which is tied to a logic '0' via resistors R060 &R061.

The YUV outputs (I038 pins 36,35,38) are terminated by resistors R021,R023 and R025 respectively. Transistors Q001,Q002, and Q003 buffer the YUV output to the monitor option shunts M100,M101 which direct either YUV - or RGB-encoded signals to the monitor output socket M016.

3.2.6 Floppy-Disc Controller (FDC)

The floppy-disc controller handles all data-transfer between the disc-drive and CPU. A maximum of four drives may be connected to the main board, two 3" micro-discs internally via M005, M008, M009 and two further 3" or 5¼" drives externally via M004 - these must be powered from a seperate external supply.

Drive Selection

Four disc-drive units may be accessed by writing the appropriate bit-pattern to the drive-select latch (I043) using the drive-select port ($\overline{DRSEL}$). Data bits 0-3 (D0-D3) control which drive is selected and bit 4 (D4) provides an optional side-select signal. The remaining data-bits D5-D7 are reserved for future expansion and have no output connection, the drive-select outputs from I043 are gated with the motor-on (MON) signal from the disc-controller (I042 pin 20) and buffered by "open-collector" NAND gates I045 to the disc-drive output plugs M004, M005. The side-select signal is buffered by I046d.

FDC-CPU Interface

All disc-drive signals are generated and interpreted by the Floppy-Disc Controller, I042, which interfaces between the CPU and disc-drives. Timing for the controller is derived from the 8MHz system master-clock and the remaining CPU interface signals except reset ie. $\overline{WR}$, A0, A1 and $\overline{FDC}$ (the port address) connect directly to the FDC. The reset pin of the FDC (pin 13, I042) is connected to the software-reset, $\overline{SFTRST}$, from the PSG. This allows the FDC to be reset by software in the event that a disc is not present in the drive selected, otherwise the FDC suspends operation until it receives a number of index pulses ($\overline{INDEX}$) from the drive. This is not always desirable as unless a disc is inserted further disc-access is not possible via the FDC. The $\overline{SFTRST}$ allows the FDC to be reset to a known condition after a suitable "timeout" generated in software.

Disc Control & Data Signals

The disc-drive(s) are controlled using 5 output and 4 input lines on the FDC. The outputs are buffered by "open-collector" NAND gates (I044, I046a) wired as inverters, these provide the necessary drive capability for the disc-drives which normally have internal 150 ohm pull-ups (Teac FD30A is exceptional having 1k ohm pull-ups fitted). Similarly the disc-drive outputs require pull-ups and these are provided by R027, R028, R030, R031.

The FDC control outputs are:-

i) Motor-On (MON; I042 pin 20); this signal is used to turn the disc-drive spindle-motor on to spin the disc.

ii) Direction (DIRC; I042 pin 17); this controls the stepping direction of the read/write head. The output (I042, pin 17) is at logic '1' to step towards the centre of the disc.

iii) Step, (STEP; I042 pin 16); this output provides pulses to move the read/write head by one track across the disc. The pulse-width is 4us. When "seeking" a particular track the period between pulses will be 12ms as set by the operating-system.

iv) Write Data (WD; I042 pin 22); this signal is the data-output to the floppy-disc. Clock and data pulses are written onto the disc using this output. The (serial) data is encoded using Modified Frequency Modulation (MFM).

v) Write Gate (WG; pin 21); this output sets this disc-drive into a write condition typically 2us prior to Write-Data becoming active

The FDC control inputs from the disc drive(s) are:

i) Track-zero ($\overline{TROO}$; I042 pin 23); this signal, which is usually derived from an opto-electronic device within the disc-drive, indicates that the read/write head has reached its outermost position on the surface of the disc. This signal appears in the status-register of the FDC and is generally used as a physical datum point for the disc-operating system (DOS) software.

ii) Write-Protect ($\overline{WPRT}$; I042 pin 25); again this is generated by an opto-electronic device positioned over the write-protect hole of the floppy disc. If the disc is "write-protected" then this input goes to a logic '0' which prevents disc write-operations from taking place. The write-protect signal also appears as a bit in the status register.

iii) Read Data ($\overline{RD}$ I042 pin 19); this is the raw data input from the disc-drive which carries both clock and data information which is then seperated within the FDC.

iv) Index Pulse ($\overline{IP}$; I042 pin 24); this pulse appears once per revolution of the disc ie. once every 200 +-4ms triggered by a hole in the disc-surface passing between an opto-electronic sensor on the drive-unit. This signal is used to sense whether or not a disc is present and spinning in the drive, it also serves as a physical datum for disc-formatting purposes.

3.2.7 Analogue-to-Digital Converter (ADC)

The Analogue-to-Digital Converter section is used to measure analogue voltages and convert these to digital (binary) quantities to be used by the CPU in control or measurement applications. There are four analogue inputs which are independently controlled by software, which can also select the particular mode in which the ADC operates.

ADC-CPU Interface

The ADC is a 20 pin dual-in-line device which fits into the centre two rows of holes (marked I050) on the printed circuit board. The ADC uses a successive - approximation technique to convert four analogue inputs to digital values. The device is selected using the decoded port-address $\overline{ADC}$ which is connected to chip-select (CS;I050 pin 2) and the Z80 read ($\overline{RD}$) and write ($\overline{WR}$) signals (I050 pins 1 and 19 respectively).

The ADC has an interrupt output ($\overline{INTR}$, I050 pin 18) which signals the end of a conversion cycle. The $\overline{INTR}$ output is taken to a gate I020d (pin 13) where it is combined with the output from an interrupt-mask latch (I51a). This allows the interrupt to be disabled by setting I051a output (pin 5) to logic '1' by writing to the $\overline{ADCINTMSK}$ port which latches data-bit D0 into I051 by combining $\overline{ADCINTMSK}$ with the Z80 write ($\overline{WR}$) signal.

The ADC interrupt is automatically disabled by the $\overline{\text{RESET}}$ signal which presets the latch output (I051a, pin 5) to logic '1' via the latch "set" ($\overline{\text{S}}$;I051, pin 4). The output from I020d (pin 11) is then fed into the interrupt logic (I033a, pin 1) - See section 2.7.

Analogue Interface

The ADC has four multiplexed analogue inputs, (I050 pin 3,4,5,6) these are connected to two external sockets, channels 1 and 2 are connected to pins 1 and 3 of M014 (ANALOGUE 1) respectively, and channels 3 and 4 to pins 1 and 3 of M015 (ANALOGUE 2) respectively. These analogue inputs have a usable input range of OV to VEF (between 1.8V and 2.1V) The reference voltage is generated by three series diodes (D001,D002, and D003) and a resistor (R037), this is smoothed by a capacitor C014 to provide a stable reference voltage.

"Fire" Button Inputs

A further connection on each analogue input socket permits the connection of a "fire" button to the computer e.g. when joysticks are used in conjunction with the analogue inputs. The "fire" inputs ($\overline{\text{FIRE1}}$ and $\overline{\text{FIRE2}}$) have pull-up resistors to the +5V power-rail, to allow the "fire" buttons to be connected between the "fire" inputs and OV. The two inputs are connected to the tri-state buffer I036 so that the state of the fire buttons may be determined by testing data-bits 0 ($\overline{\text{FIRE1}}$) and 1 ($\overline{\text{FIRE2}}$) of the I/O port $\overline{\text{KYBDINTMSK}}$.

Both "fire" button inputs are combined by I052c and then inverted by I052d to be used to generate an interrupt whenever either fire input is taken to logic '0'. This combined signal is gated in I034d by an interrupt mask signal (I051b, pin 9). The interrupt-mask is enabled either by a $\overline{\text{RESET}}$ pulse at the "set" input (pin 10) or by clocking (via I054b) a logic '1' into the latch from data-bit D0 during an I/O write operation. The output from I034d (pin 13) is then fed into the interrupt-logic (I033c pin 9).

3.2.8 Interrupt Logic

This part of the circuit provides the necessary logic to enable all of the peripheral i.c.s. under the Z80 mode 2 interrupt system. This is a "vectored" interrupt system and sufficient extra hardware has been added to enable non-Z80 family peripherals to provide the appropriate vector. Logic gates have also been included to allow a "daisy-chain" priority structure to be implemented.

Z80 Mode 2 Interrupts

When an interrupt is generated in Mode 2 the Z80 completes the current instruction and generates and Interrupt-Acknowledge (INA) signal which is the combination of the first machine-cycle (M1) signal and Input/Output Request (IORQ) signal. On receipt of an interrupt-acknowledge, the interrupting peripheral must supply an 8 bit vector via the data-bus to the CPU. This vector is then used to locate the appropriate interrupt-service routine.

"Daisy-Chain" Interrupt Priority

The interrupt-priority, when using Mode 2 interrupts, is set by gating an Interrupt Enable signal in each of the peripherals with the interrupt generated by that peripheral. The gating is arranged such that any peripheral which flags an interrupt will prevent interrupts of lower priority from being recognised by the processor. This also means that when a high priority interrupt has been serviced and interrupts re-enabled any lower-priority interrupts will be serviced in order of descending priority. At the top of the "daisy-chain" in the TC01 is the keyboard interrupt line (KYBDINT) and this is connected to the Interrupt-Enable Input, (IEI, I058, pin 13) of the Counter-Timer Circuit (CTC). Therefore, if KYBDINT becomes active (See section 3.2.4) the CTC is prevented from interrupting. If, however, KYBDINT is inactive; the CTC can interrupt the CPU at will. The CTC also has an Interrupt-Enable Output (IEO; pin 11, I058) which goes inactive - logic '0' - if the CTC has generated an interrupt, or if IEI on the CTC is at logic '0'. Thus whenever a peripheral device generates an interrupt a logic '0' ripples down the daisy-chain preventing any other device from interrupting.

The CTC Interrupt-Enable-Output (I058 pin 11,) is connected to two gates I033a and I033b, which provide the daisy-chain function from the ADC by preventing the ADCINT (ADC Interrupt) signal from reaching the Interrupt-Vector Encoder (see below) by gating using I033b and I021d. Also the daisy-chain is preserved by I033a and I021c which feeds the Interrupt-Enable-Input (IEI); I063 pin 24,) of the Parallel Input/Output (PIO) device.

Like the CTC, the PIO can only interrupt the CPU if its Interrupt-Enable Input (IEI; I063 pin 24,) is at logic '1' i.e. if no higher priority device has an interrupt pending. If IEI is at logic '0' or the PIO has an interrupt pending then the Interrupt Enable Output (IEO; I063 pin 22,) will be set to logic '0'. This signal is gated with the Fire-Button Interrupt (FIREINT) by I033c to allow a Fire-Button Interrupt only when no other device has an interrupt pending. The Fire-Button Interrupt has the lowest priority of all and so the daisy-chain is not continued beyond this point.

Interrupt-Vector Encoder

This part of the circuit generates the interrupt-vectors for the non-Z80 peripherals. The interrupt signal from each such device is fed via the daisy-chain gating to a transparent latch (IO55) which is maintained in the "transparent" state so that any interrupt generated is passed through to a priority encoder device, IO56, which encodes eight inputs to 3 binary encoded output lines. Only four of the uncoded inputs to IO56 are used (the remainder - pins 1,2,3,4, are tied to the +5V rail); when one of these inputs (IO56, pins 10,11,12,13) is taken to a logic '0' by an interrupting device the resulting encoded output (IO56, pins 6,7,9) is fed to a tri-state buffer, IO57, which writes a vector onto the data-bus. The timing of this operation is determined by the Z80 itself as follows, whenever one of the inputs to the encoder (IO56 pins 10,11,12,13) goes to logic '0' the strobe output (IO56, pin 14) is also taken to logic '0' this is buffered by IO46c and IO46d (open collector outputs) and connected to the Interrupt line ($\overline{INT}$). The strobe output (IO56 pin 14) is also used to gate (in IO54c) the Interrupt-Acknowledge ($\overline{INA}$) signal from IO54a, this ($\overline{INA}$) signal becomes active when the Z80 recognises that the $\overline{INT}$ line has become active. The output from IO54c is used both to enable the interrupt vector onto the data-bus via IO57 (pins 1,19) and to latch via IO55 (pins 4,13) the interrupt lines to ensure that this vector is not altered, by a subsequent interrupt, during the interrupt-acknowledge cycle. The vector is then read by the CPU and $\overline{INA}$ goes inactive, placing IO57 into tri-state mode and IO55 into its "transparent" state. The interrupt inputs (IO55 pins 1,2, and 6) must be reset to logic '1' by software which writes to the appropriate latch after the interrupt has been serviced.

3.2.9 Counter-Timer Circuit (CTC)

The CTC (IO58) has four counter/timer channels and these have two modes each i.e. counter and timer modes. When using the counter-mode a Down Counter is decremented by each triggering edge of the external clock inputs (CLK/TRG) of the CTC, in timer-mode the down-counter is decremented by the output of a pre-scaler (÷256) which is driven from the (4MHz) system clock.

The CTC has two functions within this system; to provide a real-time clock feature by interrupting the processor at a given interval, and to provide programmable clock-signals for the serial (RS232) interface, receive and transmit clock inputs.

CTC-CPU Interface

The CTC is mapped into a block of eight I/O address by the partially decoded port address-line $\overline{CTC}$ (IO58 pin 16). This is further decoded by the two address lines A0,A1 (IO58 pins 18,19 respectively), in conjunction with the Z80 $\overline{IORQ}$, $\overline{RD}$, and SYSCLK (IO58 pins 10,6,15, respectively). Interrupt-vector logic is included within the CTC and requires the Machine-Cycle One (M1;IO58 pin 14), Interrupt Enable In (IEI;IO58 pin 13) and Interrupt Enable Out (IEO; IO58 pin 11), $\overline{RESET}$ is also fed to the CTC.

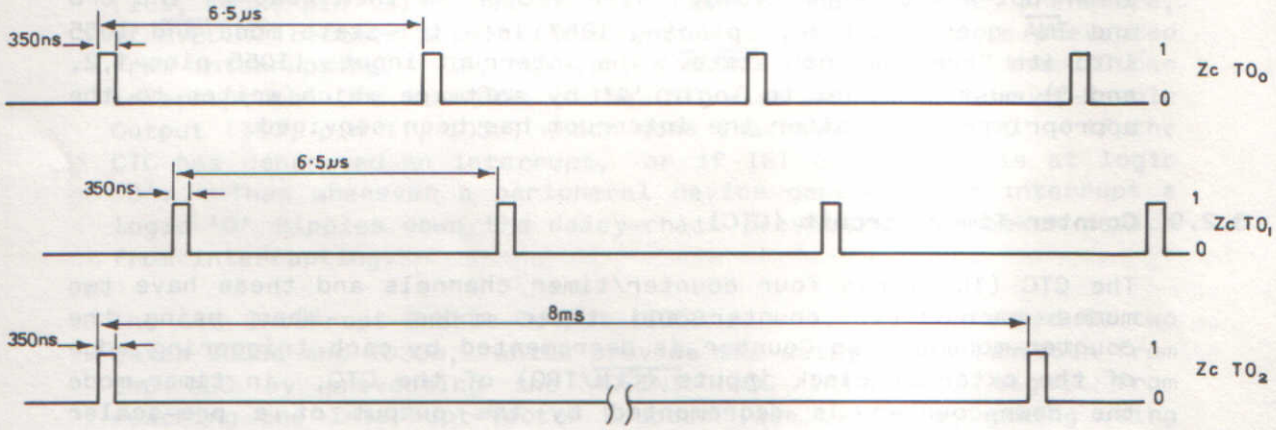
Timing Input/Outputs

Three of the timing inputs for the CTC are derived from either the system clock (4MHz) or a divided clock of 2MHz (via I058; pin 21,22 and 23) depending on the mode programmed. The fourth channel input (CLK/TRG3; I058 pin 20) is derived from the output of the third channel (ZC/TO2;I058 pin 9) these two channels provide the timing interval for the real-time clock software. When power is applied to the computer board the machine operating-system (MOS) sets the mode and selects the appropriate divide-ratio for each CTC channel.

This gives the following outputs from the CTC:-

Channel	I058 pin No.	Frequency
Channel 0	7	153.85kHz
Channel 1	8	153.85kHz
Channel 2	9 (&20)	125Hz

These are shown in Fig.3.6.'CTC OUTPUTS' below.



* SIGNALS ARE NOT SYNCHRONISED TO EACH OTHER

Fig. 3.6 CTC OUTPUTS (REAL-TIME & RS232C CLOCKS)

Channels 0 and 1 outputs (I058 pins 7,8) are connected to the serial interface to provide receive and transmit clock signals - these are set by the MOS to give a 9600 baud default transfer rate. (The frequency is internally divided by 16 in the Programmable Communication Interface ie. 153.85kHz/16 = 9600Hz). Channel 2 of the CTC has its output (I058 pin 9) connected to channel 3 input (I058 pin 20) which has no output pin but relies on interrupts to signal that zero has been reached when counting (down). The CTC is programmed by the MOS to interrupt, ie. $\overline{INT}$ goes to logic '0', at a rate of 0.5Hz - once every two seconds, the MOS then updates the real-time clock.

3.2.10 Programmable Communications Interface (PCI)

The PCI handles all serial input/output via the RS232C connector (M013). The common RS232C signals are provided directly by the PCI which also generates/strips parity bits and stop bits. The serial inputs/outputs are buffered by level-shifting devices which convert the TTL - level signals to the +- 12V levels required for the RS232C standard.

PCI-CPU Interface

The PCI is addressed via a decoded port-address $\overline{PCI}$ (I060 pin 11) address-line A0 (I060 pin 12) and the Z80 $\overline{RD}$ and $\overline{WR}$ (I060 pins 13,10 respectively) signals. Timing is derived from the master clock at a frequency of 2MHz on I060 pin 20, and the CTC outputs provide the transmit and receive clock signals at the appropriate frequency for the baud-rate required (I060 pins 9,25 respectively). The MOS software sets the clock frequency to 153.85kHz on these two connections (I060 pins 9,25).

Serial Input/Output. (RS232C)

There are four main signal connections to the PCI these comprise the Transmitted-Data (TxD) output, the Received-Data (RxD) input and two "handshaking" signals; Request-To-Send ($\overline{RTS}$) output and Clear-To-Send ($\overline{CTS}$) input these signals are buffered and connected to the RS232C socket M013. Two further modem control signals are also provided; a Data-Set Ready ($\overline{DSR}$) input, and Data-Terminal Ready ($\overline{DTR}$) output.

The Transmit-Data output (TxD; I060 pin 19) is inverted and buffered by I061a which changes the output-level (I061a, pin 3) to -12V for a logic '1' input (I061a, pin 2) and to +12V for a logic '0' input, the output from I061a (pin 3) is connected to M013 pin 3. Similarly the Request-to-Send ($\overline{RTS}$; I060 pin 23) is buffered by I061b and fed to M013 pin 4, and Data-Terminal-Ready ($\overline{DTR}$; I060 pin 24) is buffered by I061c although this has no external connection.

The serial-interface inputs are converted from +- 12V levels to TTL logic levels by a line-receiver I.C. (I062). The received data is input to the RS232C socket (M013 pin 5) and then fed to I062a (pin 1), the output of I062a (pin 3) connects to the RxD input of the PCI (I060).

The CTS signal from M013 (pin 2) is fed to I062b (pin 4) and then output (via I062b pin 6) to the $\overline{CTS}$ input of the PCI (I060). The DSR input (no external connection) is fed to I062c input (pin 10) and the output of I062c (pin 8) is connected to the $\overline{DSR}$ input of the PCI (I060 pin 22).

The spare output buffer has it inputs (I061d; pins 12,13) tied to +5V via R044, and the unused line-receiver input (I062d; pin 13) is tied to -12V via R045. A capacitor (C017, C016, C015) is connected to the response control input of each gate used in I062 (pins 2,5,9) to provide noise filtering.

3.2.11 Parallel Input/Output (PIO)

The PIO handles the parallel-printer (Centronics) interface, via the "Printer" socket (M001), and an unreserved parallel input/output port for user-defined applications, via the "User I/O" socket (M002).

PIO-CPU Interface

The PIO uses a number of the Z80 control bus signals to interface to the CPU. The PIO is addressed using the decoded port-address PIO (I063 pin 4) and two address lines A0 and A1 (I063 pins 35,36) trigger the data transfer between the CPU and PIO.

Timing for the PIO is derived from the system clock at 4MHz (I063 pin 25), and the PIO is connected into the interrupt-structure of the Z80 using the interrupt daisy-chain lines IEI and IEO; I063 pins 22,24 respectively) and the interrupt control lines INT (I063 pin 23) and M1 (I063 pin 37).

Parallel Input/Output (Printer and User I/O)

The PIO has two 8 bit parallel ports which can be used as either inputs or outputs under software control. Port A is dedicated as a printer output by the MOS at power-on, and this port has a monostable (I053b) which provides a (1us) pulse triggered by the Ready (ARDY;I063 pin 18) line of the PTO port A and is fed to the $\overline{\text{STROBE}}$ output (M001, pin 1). This pulse is needed to comply with the Centronics printer -interface timing. As well as the eight data-line outputs (I063 pins 7,8,9,10,12,13,14,15) which are fed direct to the printer connector (M001 pins 3,5,7,9,11,13,15,17 respectively). there are three "handshake" input lines from the printer connector BUSY, PAPER EMPTY, $\overline{\text{ERROR}}$ (M001 pins 21,23,28) which are connected to the tri-state buffer I036 (pins 15,13,11) to allow printer error conditions to be detected. The even-numbered pins of the printer connector (M001) are connected to 0V.

The data-lines from port B (I063 pins 27,28,29,30,31,32,33,34) are connected to the user I/O connector (M002, pins 2,4,6,8,10,12,14,16) and the Ready (BRDY; I063 pin 2) is connected to M002 pin 5. Strobe lines from each connector (M001, pin 19 and M002 pin 11) are connected to pull- up resistors R057 and R058 as well as the strobe inputs of the PIO ($\overline{\text{ASTB}}$,$\overline{\text{BSTB}}$; I063 pins 16,17 respectively)

INTEGRATED CIRCUIT DETAILS

REF	PACKAGE	TYPE	5V	0V	CAP
[illegible]001	40	Z80A	11	29	C027
[illegible]002	20	74LS244	20	10	
[illegible]003	20	74LS244	20	10	
[illegible]004	20	74LS245	20	10	
[illegible]005	20	74LS244	20	10	
[illegible]006	16	74LS157	16	8	C047
[illegible]007	16	74LS157	16	8	
[illegible]008	16	4164	8	16	C031
[illegible]010	16	4164	8	16	C032
[illegible]011	16	4164	8	16	C033
[illegible]012	16	4164	8	16	C034
[illegible]013	16	4164	8	16	C035
[illegible]014	16	4164	8	16	C036
[illegible]015	16	4164	8	16	C037
[illegible]016	16	4164	8	16	C038
[illegible]017	14	74LS32	14	7	
[illegible]018	14	74LS08	14	7	
[illegible]020	14	74LS32	14	7	
[illegible]021	14	74LS04	14	7	
[illegible]022	14	74LS00	14	7	
[illegible]023	28	2764	28	14	C062
[illegible]024	28	2764/128	24	14	C063
[illegible]025	14	74LS74	14	7	
[illegible]026	16	74LS138	16	8	
[illegible]027	16	74LS138	16	8	
[illegible]028	14	74LS02	14	7	
[illegible]030	40	AY-3-8910	40	1	C044
[illegible]031	14	74LS74	14	7	C043
[illegible]032	14	74LS32	14	7	C041
[illegible]033	14	74LS00	14	7	
[illegible]034	14	74LS02	14	7	
[illegible]035	14	74LS30	14	7	
[illegible]036	20	LS244	20	10	
[illegible]037	8	LM386	6	4	
[illegible]038	40	TMS9129	33	12	C057
[illegible]040	18	4416	9	18	C055
[illegible]041	18	4416	9	18	C056
[illegible]042	28	FD1770	15	14	C042
[illegible]043	20	74LS373	20	10	C050
[illegible]044	14	7438	14	7	C058
[illegible]045	14	7438	14	7	C061

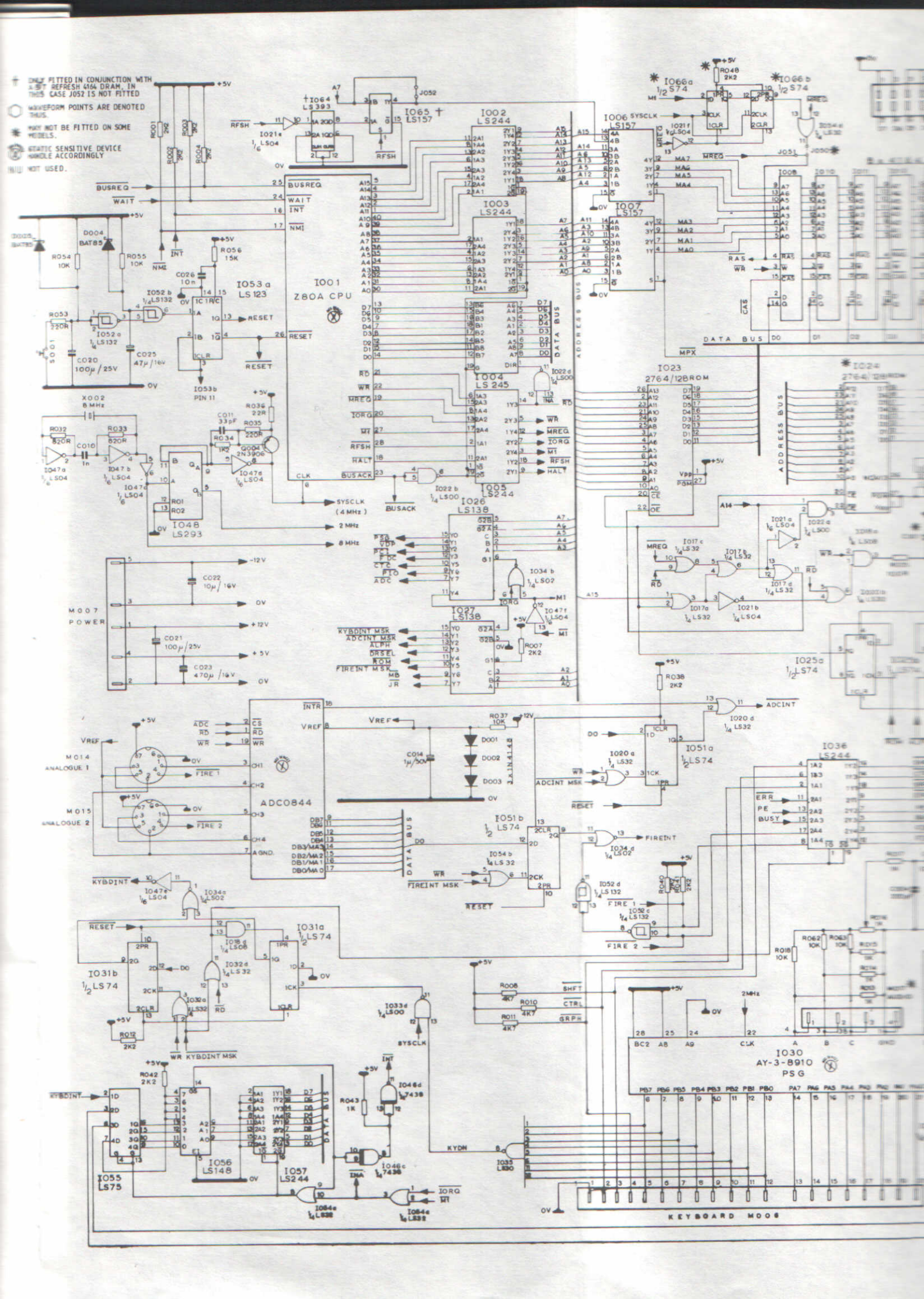
INTEGRATED CIRCUIT DETAILS

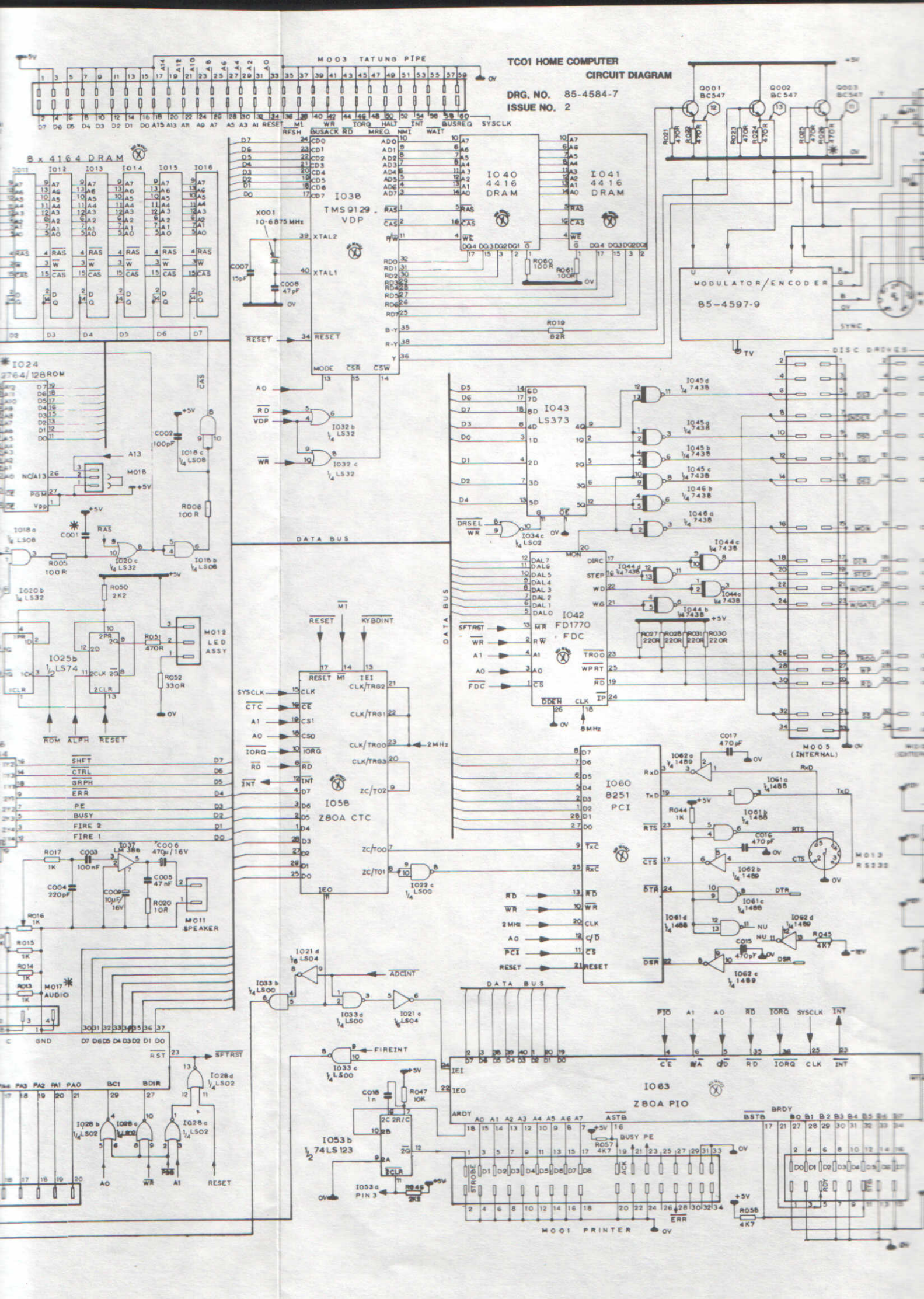
REF	PACKAGE	TYPE	5V	0V	CAP
1046	14	7438	14	7	C060
1047	14	74LS04	14	7	
1048	14	74LS293	14	7	C028
1050	20	ADC 0844	20	10	
1051	14	74LS74	14	7	
1052	14	74LS132	14	7	C030
1053	16	74LS123	16	8	C048
1054	14	74LS32	14	7	
1055	16	74LS75	16	8	C045
1056	16	74LS148	16	8	C046
1057	20	74LS244	20	10	
1058	28	Z80ACTC	24	5	C052
1060	28	8251	26	4	C053
1062	14	DS1489	14	7	C040
1063	40	Z80APIO	26	11	C051
1064	14	74LS393	14	7	
1065	16	74LS157	16	8	
1066	14	74S74	14	7	

REF	PACKAGE	TYPE	12V	0V	−12V
1061	14	DS1488	14	7	1

I/O MAP

ADDRESS (HEX)	FUNCTION
00 - 07	$\overline{\text{PSG}}$
08 - 0F	$\overline{\text{VDP}}$
10 - 17	$\overline{\text{PCI}}$
18 - 1F	$\overline{\text{FDC}}$
20	$\overline{\text{KYBDINT MSK}}$
21	$\overline{\text{ADCINT MSK}}$
22	$\overline{\text{ALPH}}$
23	$\overline{\text{DRSEL}}$
24	$\overline{\text{ROM}}$
25	$\overline{\text{FIREINT MSK}}$
26	
27	
28 - 2F	$\overline{\text{CTC}}$
30 - 37	$\overline{\text{PIO}}$
38 - 3F	$\overline{\text{ADC}}$


† ONLY FITTED IN CONJUNCTION WITH A 5T REFRESH 4164 DRAM. IN THIS CASE J052 IS NOT FITTED
WAVEFORM POINTS ARE DENOTED THUS.
* MAY NOT BE FITTED ON SOME MODELS.
STATIC SENSITIVE DEVICE HANDLE ACCORDINGLY
NOT USED.
IO01 Z80A CPU
IO02 LS244
IO03 LS244
IO04 LS 245
IO05 LS244
IO06 SYSCLK LS157
IO07 LS157
IO08
IO09
IO10
IO23 2764/128ROM
IO24 2764/128ROM
IO25a 1/2 LS74
IO26 LS138
IO27 LS138
IO30 AY-3-8910 PSG
IO31a 1/2 LS74
IO31b 1/2 LS74
IO36 LS244
IO48 LS293
IO51a 1/2 LS74
IO51b 1/2 LS74
IO52 b 1/4 LS132
IO52 a 1/4 LS132
IO52 c 1/4 LS132
IO52 d 1/4 LS132
IO53a LS 123
IO53b PIN 11
IO55 LS75
IO56 LS148
IO57 LS244
IO64 LS 393
IO65 † LS157
IO66a 1/2 S74
IO66 b 1/2 S74
M007 POWER
M014 ANALOGUE 1
M015 ANALOGUE 2
ADC0844
KEYBOARD M006
BUSREQ
WAIT
INT
NMI
RESET
BUSACK
SYSCLK (4 MHz)
2 MHz
8 MHz
ADDRESS BUS
DATA BUS
FIRE 1
FIRE 2
FIREINT
KYBDINT
KYBDINT MSK
FIREINT MSK
ADCINT
SHFT
CTRL
GRPH
PSG


TC01 HOME COMPUTER
CIRCUIT DIAGRAM
DRG. NO. 85-4584-7
ISSUE NO. 2
M003 TATUNG PIPE
8 x 4164 DRAM
IO38 TMS9129 VDP
IO40 4416 DRAM
IO41 4416 DRAM
MODULATOR/ENCODER
85-4597-9
IO24 2764/128 ROM
IO43 LS373
IO42 FD1770 FDC
IO58 Z80A CTC
IO60 8251 PCI
IO63 Z80A PIO
IO53b 74LS123
M001 PRINTER
M005 (INTERNAL)
M012 LED ASSY
M011 SPEAKER
M013 RS232
DATA BUS
DISC DRIVES

4. PAL ENCODER AND RGB MATRIX

4.1. GENERAL

The PAL encoder and RGB Matrix circuitry described following is housed on the computer's main P.C.B. assembly.

The physical location of these section is shown in Fig.3.3 'PCB FUNCTIONAL BLOCK LAYOUT'; in SECTION 3.

4.1.1 Circuit Diagram

The circuit descriptions following should be read in conjunction with the circuit diagram for the 'TCO1 RGB/PAL ENCODER AND UHF MODULATOR' - Drawing No. 85-4597-9.

Waveforms shown in diagrams accompanying this section, were measured at points shown thus ⟨14⟩ on the circuit diagram.

4.2 PAL ENCODER

4.2.1 Circuit Details - General

The PAL encoder provides a composite video signal and feeds the UHF modulator. This generates an R.F. (UHF) output signal for feeding a receiver/monitor display unit at a line impedance of 75ohms.

The PAL encoder comprises:-

Chroma encoder.

PAL switch.

PAL switch signal generator.

SYNC pulse separator.

Subcarrier oscillator.

Adder.

4.2.2 Circuit Descriptions

Circuit details of the composite sections of the PAL encoder are described following.

4.2.3 Input Signals

The input signals R-Y and B-Y are fed to I105 (LM1889) via capacitors C116, and C114 respectively.

4.2.4 Chroma Encoder

The encoder IC, LM1889 (I105), consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma modulators, two RF oscillators and modulator for two low - VHF channels. In this application however, only the chroma subcarrier oscillator and quadrature chroma modulator are used.

A subcarrier at 4.433MHz, is fed into pins 1 and 18, such that they have a relative phase difference of 90°. When pins 1 & 3 and pins 3 & 4 have the same applied potential, there is no output from pin 13 (chroma subcarrier).

If the potential on pin 2 is more positive than pin 3, then the output on pin 13, is a 4.433MHz signal in phase with that on pin 1.

However, if the potential on pin 2 is less positive than on pin 3, then the output on pin 13 is a 4.433MHz signal 180° in antiphase to that on pin 1. The amplitude of the signal from pin 13 is then proportional to the potential difference between pins 2 and 3.

In the same way, if pins 2 & 3 are now maintained at the same potential and the potential on pins 2 & 4 are varied as above, a subcarrier signal will appear at pin 13, but the phase will be relative to pin 18.

When signals are applied to both V and U modulators simultaneously, the output on pin 13 will be the vector sum of the output of both modulators.

In operation, the U & V signals from the TMS9129 are A.C. coupled respectively, to pins 2 & 4 of I105 (LM1889). The signals are d.c. restored to +6v during the line synchronising period. (The U & V signals are shown in Fig.12 & 13 TR.1 b & c)

The d.c. reference input to the modulators (pin 3, I105), is fixed at +6v by means of the potential divider formed by R158 and R160. This ensures, that the d.c. chroma reference, is independent of any differential tolerance of U & V within the video display processor IC (TMS9129).

4.2.5 PAL Switch

The PAL switch circuit, consists of an inverter Q124 and two analogue switches I104c & d. The non-inverted subcarrier reference signal is taken from the emitter of Q124 via C125 and I104d, while the inverted subcarrier reference signal is taken from collector via C124 and I104c.

The subcarrier signal from the crystal X100, is fed into a 45° phase lead network formed by R170, R171 and C127, which feeds the base of Q124. The signal from X100, also feeds a 45° phase lag network formed by R173 and C130.

The collector and emitter loads (R166 and R167) of Q124 are chosen such that equal amplitude, but antiphase subcarrier signals, are present at the inputs to the PAL switch I104c & d. The action of the phase lead and lag networks produces a subcarrier signal on the emitter of Q124, which leads in phase; the signal on pin 18 of I105 by 90°.

Similarly, the signal on the collector, leads in phase, the signal on pin 18 of I105 (U subcarrier input) by 270°. The correct subcarrier phase for the V modulator is selected by the PAL switch I104c & d.

The control signals, PAL SW (104c) and PAL SW (104d), are in antiphase so only one signal is presented to pin 1 (I105) at a time. The switch changes the phase to pin 1 (I105) on each alternate line.

PAL switch signal generator

The PAL switch signal generator, is formed by the D type Flip-Flop (part of I103, MC14013) connected as a bistable.

The bistable is fed by line synchronising pulses, derived from the video signal, by Q123. The output is a 7.8KHz square wave (half line frequency) on pins 13 and 12 of I103a. These drive the PAL switches of I104d and I104c via pins 12 and 6.

4.2.6 SYNC pulse separator

The luminance and chrominance d.c. clamps (I102c & d, I104a & b) are restored to the chroma bias reference level (+6v) during the line flyback period. The clamps are driven by the mixed sync signal, which is separated from the luminance (Y) signal, by the sync pulse separator Q123.

The incoming luminance signal, charges C115 such that, Q123 is cut off during most of the luminance input; except during sync pulse tips. The sync pulse tips turn on Q123, producing a mixed sync output on the collector. This output is also used as the clamp pulse of I202a & b, and I104a & b. The sync pulse is used to trigger the PAL SW signal generator and clamp pulse generator of I103a & b. (shown in waveform 14).

4.2.7 Subcarrier oscillator

A crystal-controlled oscillator is used to ensure the accuracy and stability required of the subcarrier frequency for use with colour TV receivers.

The subcarrier oscillator consists of a oscillator stage in the LM1889 and an external RC circuit and crystal. The feedback signal from the crystal X100 is via the 45° lag network formed by R173, C130 and is fed to pin 18. The trimming capacitor C131 is used to adjust the subcarrier frequency to 4.433619 MHz.

4.2.8 Adder

The luminance signal from Q003 emitter (See waveform 11) is reduced in amplitude by R105 & R106 which also act as the emitter load for the luminance emitter follower have Q003. It is AC coupled to the adder Q125, by C118. R165 and C123 limit the risetime of the luminance signal.

The clamp circuit charges the capacitor C118 to +6v during the synchronising period, providing the same dc bias as on pins 2,3, and 4, of I105 for the adder Q125.

The luminance signal is then summed with the chrominance signal at Q125 via L101, C122. These form a bandpass filter for the chrominance channel, attenuating harmonics and sidebands which are outside the usable frequency spectrum of the PAL subcarrier system. The composite video appears across R168.

4.2.9 UHF Modulator

The UHF modulator consists of a dc clamp circuit I104a, a buffer Q126 and a high performance UHF modulator UM1286.

The inputs of UM1286, include fine tune, audio, Vcc and video. The fine tune and audio inputs are maintained at +5v via R177.

The composite video, is AC coupled to the output stage Q126, via C128. The capacitor C128, is charged to +1.4v by the voltage divider R172 & R174 via I104a during the line synchronising period, and provides a suitable luminance level to Q126 and the UM1286 modulator. See waveform 20.

The UM1286 modulates the composite video signal on to a channel 36 UHF carrier.

The output signal specifications are:-

1. Vision carrier Ch36 (591.25 +or- 6 MHz)
2. RF output voltage 1.0mV +or-6dB
3. RF output impedance 75 ohms

4.3. RGB MATRIX

4.3.1 Circuit Description - RGB Matrix

The circuit details for the RGB matrix are included on the circuit diagram. Input signals V and U are A.C. coupled to I101 via C102 and C103 respectively.

The signals are d.c. restored to + 3.2v during the blanking period. The luminance signal, Y, is d.c. coupled to the matrix. (A block diagram is shown in Fig. 4.1).

4.3.2 RGB Matrix

Three similar circuits are used for the RGB Matrix, each functioning as a differential amplifier. The R matrix circuit, is formed by Q110, Q111 and associated circuitry. The output signal is developed across the load resistor R121, signal amplitude being proportional to the ratio of collector resistor (R121) and emitter resistors (R122, R123, & R132).

Consider the (-R) matrix. If only (V) colour difference signal is fed to the base of Q110, and there is no luminance (Y) applied to the base of Q111, the differential amplifier acts as a single stage inverter. Similarly if only (Y) is fed to the base of Q111 then -Y is developed across R121.

When signals are applied to both inputs simultaneously, the current flow in R121 will be the sum of both collector currents, the resultant voltage drop on R121 then being taken out and used as the output signal of the R matrix.

This is shown as:-

$$\begin{aligned} E_R &= (-(R-Y)) + (-(Y)) \\ &= (-R+Y) + (-Y) \\ &= -R+Y-Y \\ &= \underline{-R} \end{aligned}$$

Similarly, for the (-B) matrix, U is fed to the base of Q114, Y is fed to the base of Q115. The output signal (-B) is taken from the collector load R126. The gain of the (-B) matrix is made larger than the (-R) matrix to compensate for the weighting of the (R-Y) and (B-Y) signals within the video display processor.

In the (-G) matrix circuit, Y is fed to the base of Q113. The -(G-Y) signal is produced by the addition of the V & U signals, and AC coupled to the emitter of Q112. (Where V is taken from the emitter of Q110 via R131 & C108, the U signal is taken from the emitter of Q114 via R134 & C110)

Otherwise; operation of the (-G) matrix, is the same as for (-B) and (-R) matrices.

This is shown as:-

$$\begin{aligned} E_V &= (-(G-Y)) + (-(Y)) \\ &= -G + Y-Y \\ &= -G \end{aligned}$$

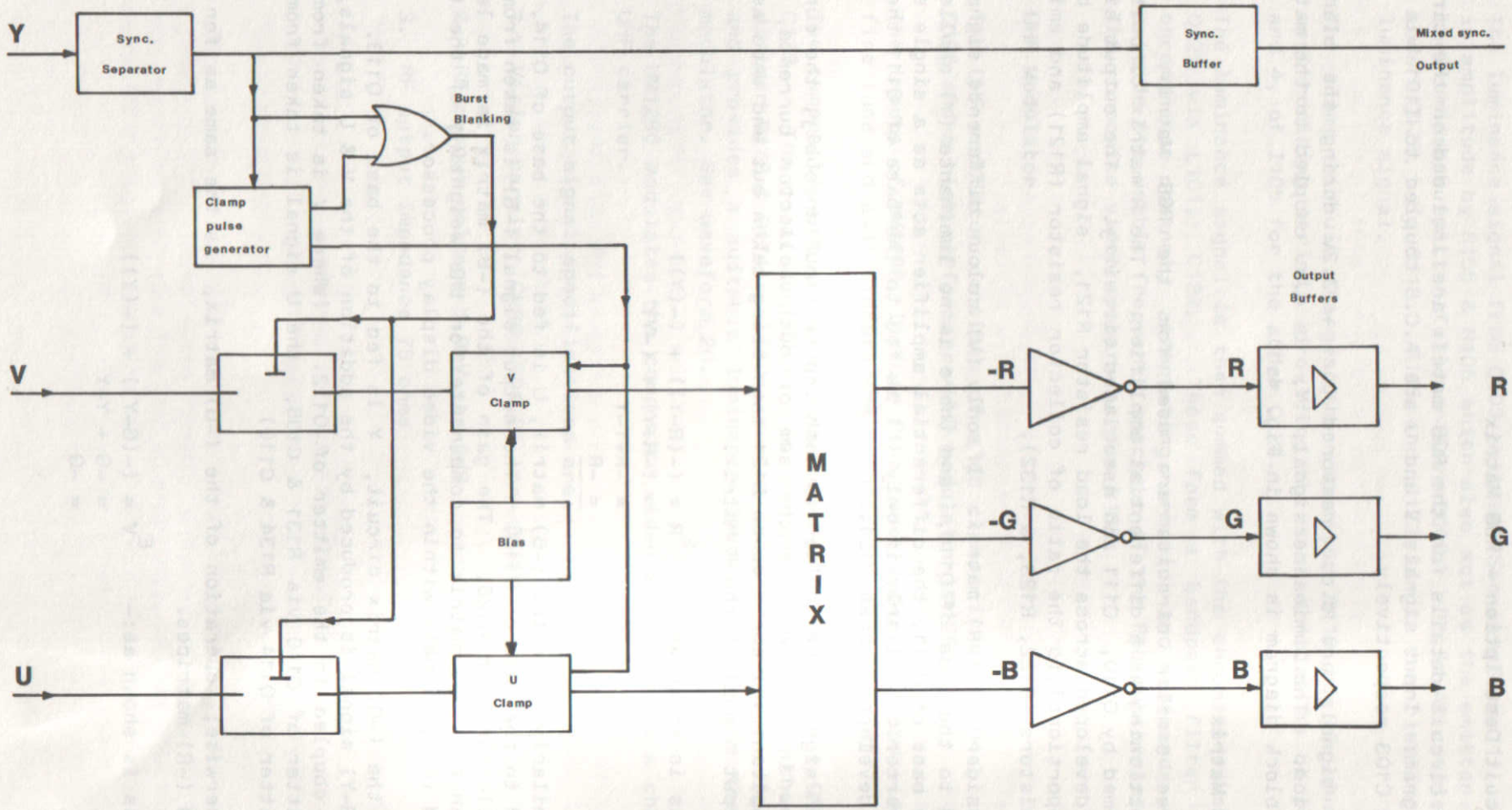


Fig. 4.1 RGB MATRIX - BLOCK DIAGRAM

4.3.3 Clamp Pulse Generator

The CLAMP PULSE generator consists of I103a (½ Integrated circuit MC14013) and R179 and C120.

The I103a is connected as a positive edge triggered monostable having a period of 9 uS.

An integrator; formed by R179 and C120 is connected between the output (pin 1) and the reset (pin 4) of I103a. The set pin (pin 6) is grounded.

At each positive edge of the clock signals, the data on pin 5, (a'1'), is delivered to the output, pin 1. The state of pin 1 is then changed from a '0' to a '1'

The voltage (+12v) on pin 1 will charge the capacitor C120 via

R179. The charged curve is $V\ (1-e^{t/CR})$ where R & C are R179, C120 respectively, V is the voltage on pin 1.

After 9 uS, the voltage on C120 will reach approximately +6v and will turn on the reset (pin 4), force the output to change state from +12v to 0v. The capacitor C120 will then discharge through R179 and pin 1. R179 may be adjusted to set the period of the monostable.

The whole operation repeats when the next clock signal appears (The waveform is shown in waveform 15).

4.3.4 Burst Blanking

The TMS9129A generates a burst gate pulse on the back porch of the video signal. This pulse is utilised by the PAL encoder, I105, but must be removed prior to matrixing, since it does not form part of the R.,G., or B signals.

The blanking signal is generated by feeding the sync and negative-clamp pulse to an 'OR' gate. (Waveform Fig. 16)

4.3.5 RGB Inverter

Transistors Q116, Q117, Q118 are inverting amplifiers with a voltage gain of 2. Each inverter has a common base bias. The input signals (-R,-G,-B) are A.C. coupled to their respective bases. The output signals are taken from the collectors.

4.3.6 RGB Output (Buffer)

Three emitter-followers Q120, Q121, Q122 are used to buffer the R.G.B. signals. Each stage provides the impedance matching function, by changing the impedance from high (input) to low (output), in order to be able to drive long connecting cables without degradation of signals. See Fig. 17, 18, 19.

4.3.7 Sync Pulse Inverter and Buffer

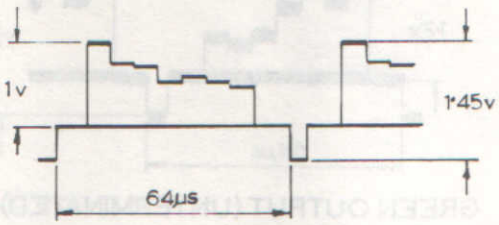
The mixed sync signal is taken from sync separator Q109 and d.c. coupled to the inverter Q108.

The negative-going sync signal is taken from the junction of R136 & R137.

4.4. WAVEFORM DISPLAYS - PAL ENCODER AND RGB MATRIX

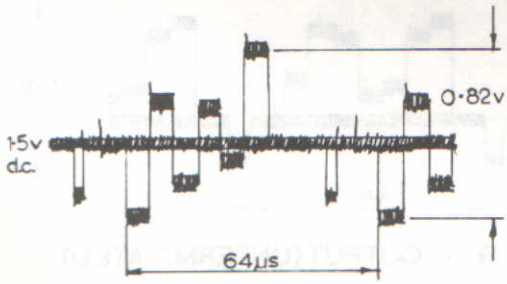
These waveform displays should be used in conjunction with the circuit diagram for the 'TC01 RGB/PAL ENCODER AND UHF MODULATOR - Drawing No. 85-4597-9.

11



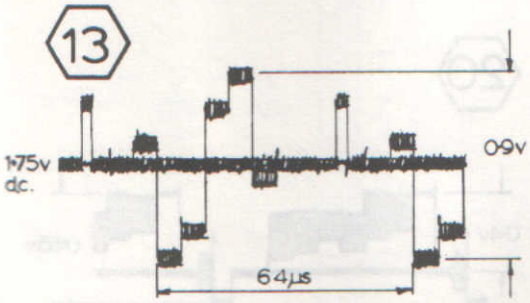
Y OUTPUT

12



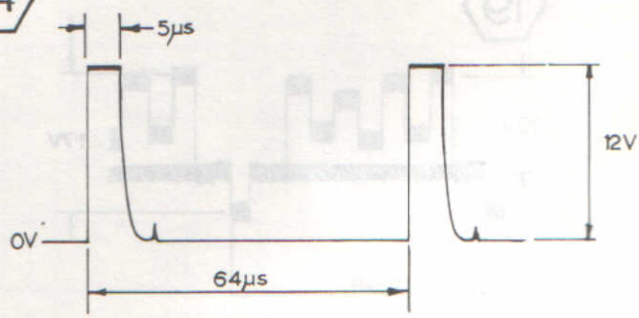
B-Y OUTPUT

13



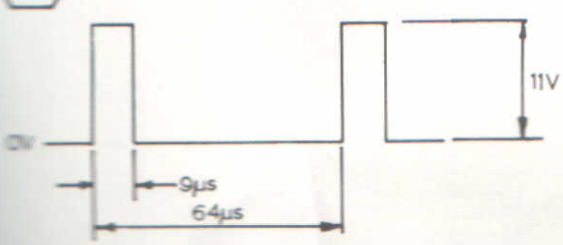
R-Y OUTPUT

14



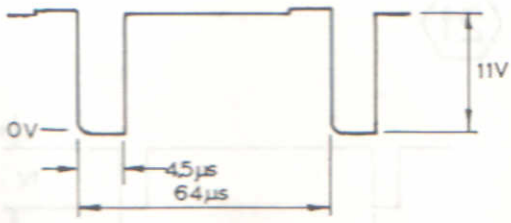
SEPERATED SYNC.

15



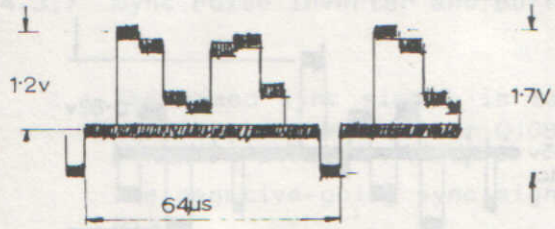
CLAMP PULSE

16



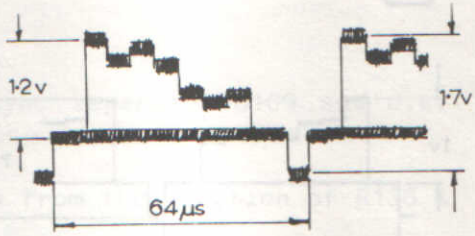
BURST GATE PULSE

17



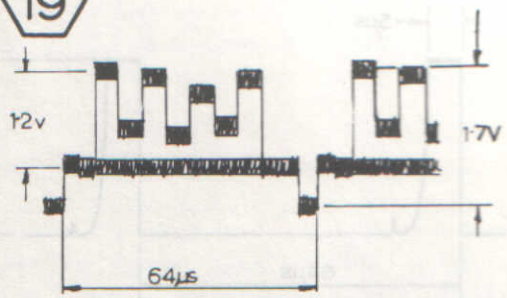
RED OUTPUT (UNTERMINATED)

18



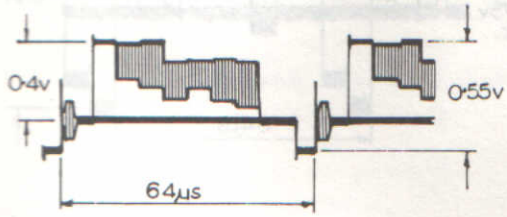
GREEN OUTPUT (UNTERMINATED)

19



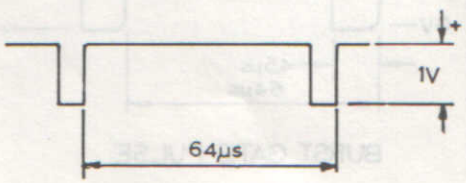
BLUE OUTPUT (UNTERMINATED)

20

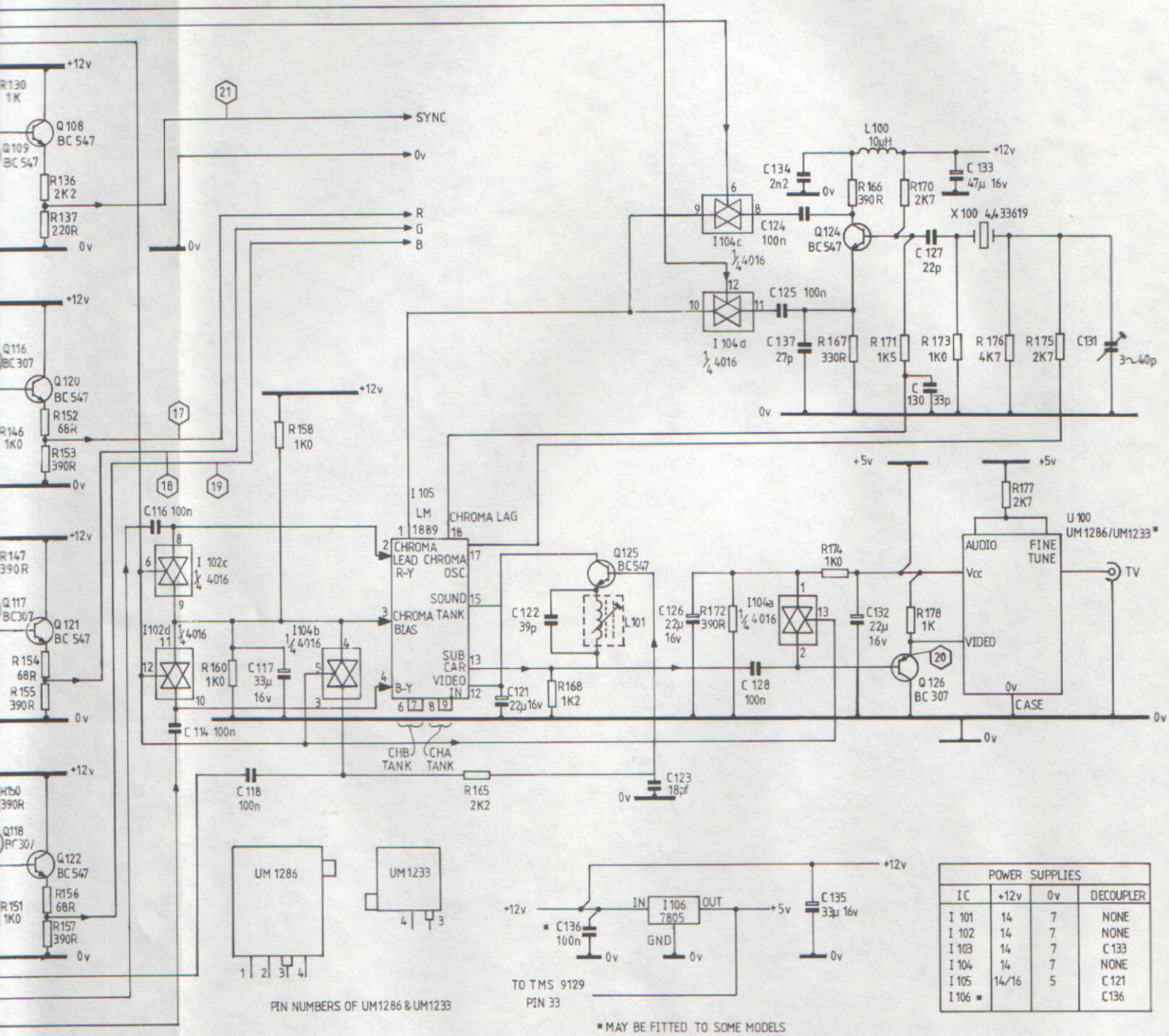


COMPOSITE VIDEO

21



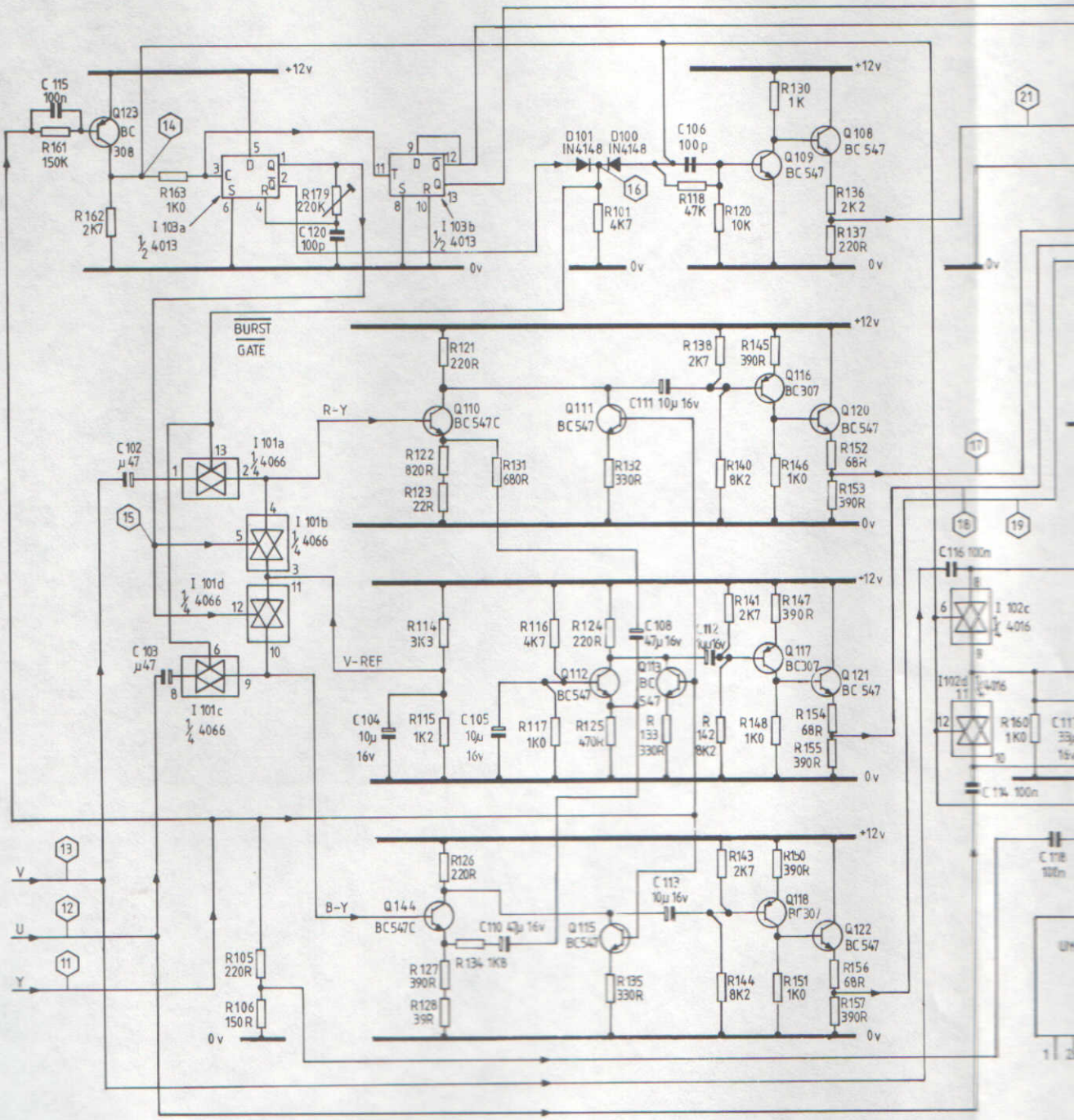
SYNC.OUTPUT



POWER SUPPLIES			
IC	+12v	0v	DECOUPLER
I 101	14	7	NONE
I 102	14	7	NONE
I 103	14	7	C133
I 104	14	7	NONE
I 105	14/16	5	C121
I 106 *			C136

NOTE:
WAVEFORM POINTS ARE DENOTED THUS: (13)
SIGNAL DIRECTION IS INDICATED THUS: →

DRAWING No. 85-4597-9



TC01 RGB/PAL ENCODER & UHF MODULATOR

5. SWITCHED-MODE POWER SUPPLY UNIT

5.1. GENERAL

The power supply incorporated is a self-contained screened, switched mode unit.

Constructed to meet BS:415:1979 requirements for Class 1 apparatus, it is provided with an electrial safety earth connection marked ⏚. After any service, ensure that original earth connections to this point are replaced and make secure contact. This is required in order to meet safety regulations, but is also of great importance to help prevent electrical radiation and provide good electrostatic screening.

Low voltage output connections are made via a flying-lead set and single multi-way connection M007 to the main computer PCB.

5.2. MAINS LEAD CONNECTIONS

If the socket outlets to be used are not suitable for the plug supplied with the computer it should be cut off and an appropriate three pin plug fitted.

NOTE: The plug severed from the mains lead must be destroyed, as a plug with bared flexible cord is hazardous if engaged in a live socket outlet.

The main lead contains three wires coloured in accordance with the following code:-

BLUE - Neutral
BROWN - Live
GREEN WITH YELLOW STRIPE - Earth

The colours of these wires may not correspond with the coloured markings identifying the terminals of your plug, therefore **CONNECT AS FOLLOWS:-**

The wire coloured BROWN must be connected to the terminal marked L or coloured RED.

The wire coloured BLUE must be connected to the terminal marked N or coloured BLACK.

The wire coloured GREEN AND YELLOW must be connected to the terminal marked E or coloured GREEN, or coloured GREEN AND YELLOW, or marked with the earth symbol ⏚.

Use a 3 amp fuse approved by ASTA to BS1362.

Always replace the fuse cover, never use the plug with the fuse cover omitted.

WARNING:- THIS APPLIANCE MUST BE EARTHED.

5.3 CIRCUIT DIAGRAM & DESCRIPTION

The circuit descriptions following, should be read in conjunction with the 'Switched-Mode Power Supply' Circuit Diagram Drg. No. 85-4666-5. Waveforms shown in the accompanying diagrams were measured at the points denoted thus ⟨E3⟩ on the circuit diagram.

5.3.1 Circuit Description

The power supply is a self-oscillating switching type of converter which, under normal conditions, operates at a free-running frequency of between 20 and 40KHz. All control functions are performed within IE01 (TDA4600-2D).

The switching transistor, QE01, switches the primary winding of the transformer TE01 across the rectified mains voltage developed on the reservoir capacitor CE02. The output voltages (5V, 12V and -18V) are generated at taps on the primary winding and rectified and smoothed by DE13, DE11, DE12, CE16, CE12, CE21, CE22 and CE18. The -12v O/P is regulated from the -18v rail by IE02, it has a current limit of approximately 150mA and thermal shutdown in the event of a continuous excessive load.

The base drive for QE01 is generated in IE01, the current at pin 8 controlling the switch-on period and that at pin 7 controlling the turn-off conditions of QE01.

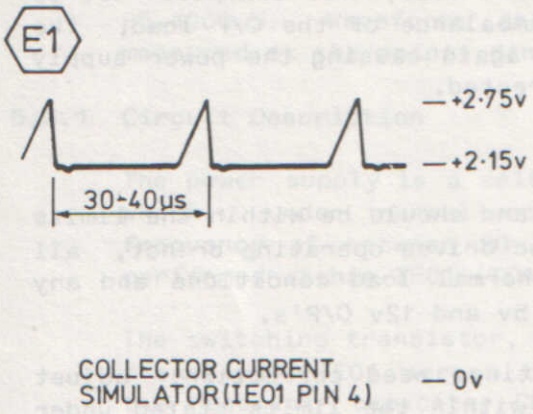
RE08, RE10 and CE08 develop a sawtooth voltage at pin 4 which simulates the collector current of QE01. This is used to generate a sawtooth base drive at pin 8 to avoid over-saturation of QE01.

DE08 and CE10 rectify and smooth a voltage from the feedback winding on TE01 which is proportional to the output voltages. In addition to the feedback through the transformer, dc feedback is arranged through the long tailed pair QE02 and QE03 via the opto-isolator KE01, which compensates for the voltage drop across DE11 and DE13 varying with different loads. The reference voltage is attenuated by RE12, RE07 and RE06 with respect to a reference voltage at pin 1 and applied to pin 3. Any changes in the output are thus transmitted via pin 3 to the control logic and the base current amplifier within the I.C. In this way the frequency and duty cycle of the output pulses are adjusted to correct for the changes.

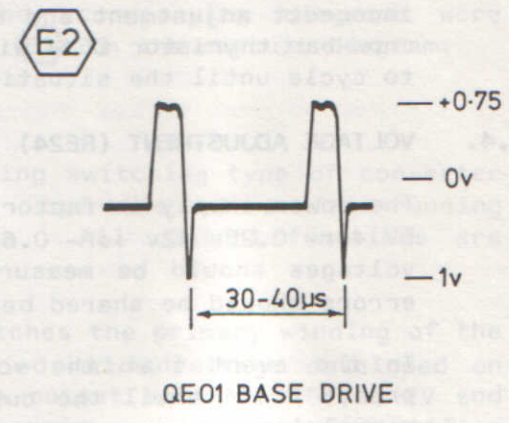
RE24 (set 5v and 12v) adjusts the proportion of voltage fed back via Amplifier (QE2,QE03) and opto-isolator KE01, and hence adjusts the output voltage. In order to complete the oscillator feedback loop, RE14 feeds an attenuated voltage from the feedback winding on TE01 to pin 2. This enables the I.C. to identify the points at which the output pulse crosses the zero voltage level and so provide correctly timed base drive pulses to QE01.

5.5. WAVEFORMS - Switched Mode Power Supply

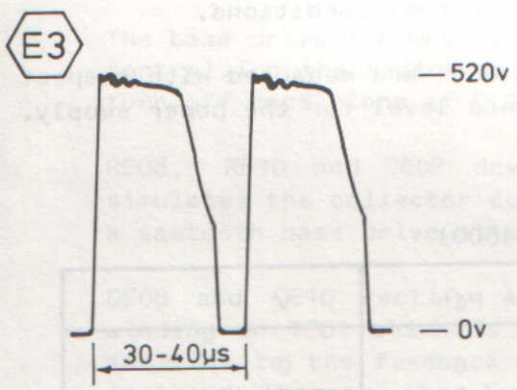
These waveform displays should be used in conjunction with the circuit diagram 'Switched Mode Power Supply' - Drawing No. 85-4666-5



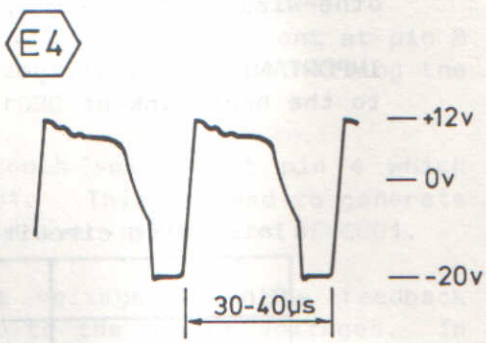
COLLECTOR CURRENT SIMULATOR (IE01 PIN 4)



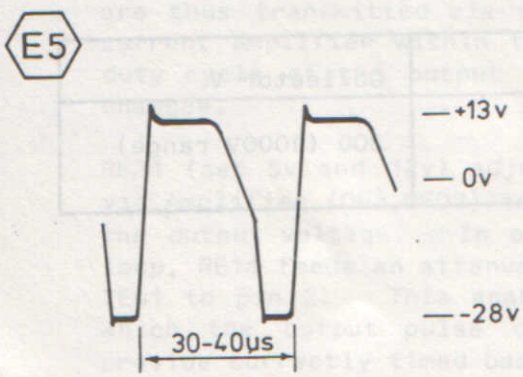
QE01 BASE DRIVE



QE01 COLLECTOR

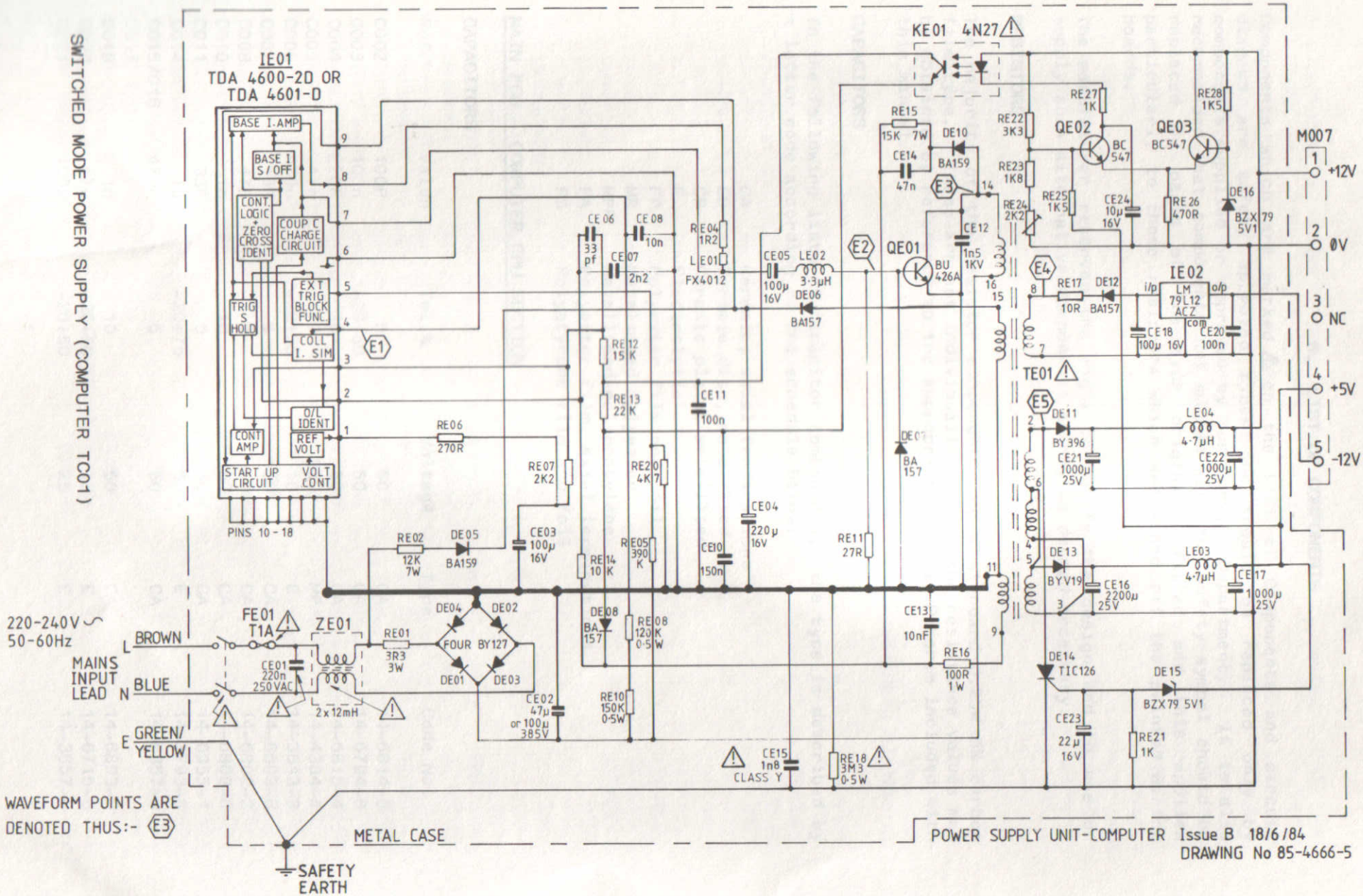


DE12 CATHODE



DE11 ANODE

SWITCHED MODE POWER SUPPLY (COMPUTER TC01)



6. LIST OF COMPONENTS

Components which are marked ⚠ on the List of Components and circuit diagams are safety approved types and should be replaced only by components supplied or approved by our Service Department. It is also recommended that components not marked with the safety symbol should be replaced by parts of the type originally fitted and this applies particularly to those resistors which are stood off the printed wiring boards.

The manufaturer reserves the right to modify the design and to use or supply such alternative components as may be deemed necessary.

RESISTORS

The majority of the resistor components are a standard 0.25W 5% carbon film type. These are not individually listed; the resistance values may be obtained by reference to the appropriate Circuit Diagram included with this manual.

CAPACITORS

In the following lists of capacitor components, the type is described by a letter code according to the schedule below:

CA	Ceramic, axial terminations
CD	Ceramic disc, metallised
CP	Ceramic plate, metallised
E	Electrolytic
FP	Polyester film and foil
MP	Metallised polyester
MPP	Metallised polypropylene
PA	Polyester film, axial terminations
PS	Polystyrene film and foil

MAIN PCB - COMPUTER CPU SECTION

CAPACITORS

Ref.	Value	Tol.%	Voltage	Type	Code No.
C002	100P	5	50	CA	14-6814-6
C003	100n	-20+80	50	CA	14-6794-8
C004	220P	10	50	CA	14-6815-4
C005	47n	20	250	MP	14-4384-4
C006	470u	-20+50	16	E	14-3843-3
C007	15P	5	50	CA	14-6603-8
C008	47P	5	50	CA	14-6802-2
C010	1n	10	50	CA	14-6803-0
C011	33P	5	50	CA	14-6355-1
C014	1u	-20+75	50	E	14-2793-8
C015/016	470P	5	50	CA	14-6357-8
C017					
C018	1n	10	50	CA	14-6803-0
C020	47u	-20+50	16	E	14-6715-8
C021	100u	-20+50	25	E	14-3657-0

Ref.	Value	Tol.%	Voltage	Type	Code No.
C022	10u	-20+50	16	E	14-3620-1
C023	470u	-20+50	16	E	14-3843-4
C025	22u	-20+50	16	E	14-2821-7
C026	10n	20	25	CA	14-6359-4
C027/028/ 030/031/032 033/034/035 036/037/038 040/041/042 043/044/045 046/047/048 050/051/052 053/054/055 056/057/058 060/061/062 063	100n	-20+80	50	CA	14-6794-8

INTEGRATED CIRCUITS

Ref.	Type and Description	Code No.
I001	Z8400A	19-8099-8
I002/003	74LS244	19-8090-4
I005	74LS244	19-8090-4
I004	74LS245	19-8091-2
I006/007	74LS157	19-4867-9
I008/010		
I011/012	4164-150	19-8096-3
I013/014		
I015/016		
I017/020	74LS32	18-2182-2
I018	74LS08	19-8083-1
I021	74LS04	19-7990-6
I022	74LS00	19-4719-2
I023	2764	19-8097-1
I025	74LS74	19-8007-6
I026/027	74LS138	19-8087-4
I028	74LS02	19-8006-8
I030	AY-3-8910	19-8100-5
I031	74LS74	19-8007-6
I032	74LS32	18-2182-2
I033	74LS00	19-4719-2
I034	74LS02	19-8006-8
I035	74LS30	19-8085-8
I036	74LS244	19-8090-4
I037	LM386	19-8095-5
I038	TMM9129 TEXAS	19-8113-7
IC040/041	4416-15NL	19-8114-5
I042	WD1770-PH	19-8110-2
I043	74LS373	19-8126-9
I044/045/046	7438	19-8127-7
I047	74LS04	19-7990-6
I048	74LS293	19-8023-8
I050	ADC044CCN NAT.SEMI.	19-8159-5
I051	74LS74	19-8007-6

Ref.	Type and Description	Code No.
I052	74LS132	19-8002-5
I053	74LS123	19-8039-4
I054	74LS32	19-2182-2
I055	74LS75	19-8086-6
I056	74LS148	19-8089-0
I057	74LS244	19-8090-4
I058	Z8430A	19-8102-1
I060	uPD8251A	19-8104-8
I061	DS1448	19-8105-6
I062	DS1489	19-8106-4
I063	Z8420A	19-8101-3

TRANSISTORS

Ref.	Type and Description	Code No.
Q001/002/003	Gen.Purpose NPN (Typical BC547)	19-5780-5
Q004	2N3906	19-7154-9

DIODES

Ref.	Type and Description	Code No.
D001/002/003/004	1N418	19-3992-0

XTALS

Ref.	Type and Description	Code No.
X001	10.738635 MHz Crystal	16-1902-0
X002	8.0 MHz Crystal	16-1903-9

CONNECTORS

Ref.	Description	Code No.
M001/M004	Conn.34-way 90° plug M52-1234-460 Pye Conn.	22-8072-8
M002	Conn.16-way 90° plug M52-1216-460 Pye Conn.	22-8069-8
M003	Conn.60-way 90° plug M52-1260-460 Pye Conn.	22-8073-6
M005	Conn.34-way plug M52-1234-250 Pye Conn.	22-8074-4
M006	Conn.20-way plug SE20/3720 Nat. Pressac	22-8079-5
M007	Conn.5-way plug SE220/1545 Nat. Pressac	22-6011-5
M008/009	Conn.4-way plug SE220/1544 Nat. Pressac	22-6047-6
M011	Conn.2-way plug SE20/3702 Nat. Pressac	22-8029-1
M012	Conn.3-way plug SE20/3703 Nat. Pressac	22-8078-7
M013	Socket 5-Pin Din 45327.3/3-3671	22-8080-9
M014/015	Socket 7-Pin Din 45329.3/3-2471	22-8082-5
M016	Socket 6-Pin Din 45322.3/3-3121	22-8081-7
M018	Conn.3-way plug 22-03-2031 Molex	22-8076-0
M018A	Conn.2-way shunt 15-38-1024 Molex	22-8077-9
I023A/024A	I.C. 28-way Mounting Socket	25-2017-6

MISCELLANEOUS

Ref.	Description	Code No.
R016	Pot.linear 1K 20% with 20mm knurled spindle	12-3156-1
S001	Reset Switch Petrick 314.01 Eurocomp.	20-4057-3
S001A	Button-Type FSC Grey ITT	25-2023-0
DL01	LED. SR632D NEC.	19-8130-7
DL02	LED. SG232D NEC.	19-8131-5

MAIN PCB - MODULATOR/ENCODER SECTION

CAPACITORS

Ref.	Value	Tol.%	Voltage	Type	Code No.
C102/103	0.47u	-20+75	50	E	14-6712-3
C104/105	10u	-50+20	16	E	14-3620-1
C106	100P	5	50	CA	14-6814-6
C108/110	47u	-50+20	16	E	14-6715-8
C111/112					
C113	10u	-50+20	16	E	14-3620-1
C114/115					
C116/118	100n	-20+80	50	CA	14-6794-8
C117	33u	-50+20	16	E	14-6819-7
C120	100P	5	50	CA	14-6814-6
C121	22u	-50+20	16	E	14-2821-7
C122	39P	5	63	CP	14-4582-0
C123	33P	5	63	CP	14-3761-5
C124/125					
C128	100n	-20+80	50	CA	14-6794-8
C126/132	22u	-50+20	16	E	14-2821-7
C127/130	33P	5	63	CP	14-3761-5
C133	47u	-50+20	16	E	14-6715-8
C134	2n2	-20+80	400	CD	14-4322-4
C135	47u	-50+20	16	E	14-6819-7

INTEGRATED CIRCUITS

Ref.	Type and Description	Code No.
I101	IC4066B	19-8122-6
I102/104	IC4016B	19-8121-8
I103	IC4013B	19-8123-4
I105	LM1889	19-8119-6
I106	LM7805	19-8129-3
I06A	HEATSINK F9-4-220: STAVER	25-2022-2

TRANSISTORS AND DIODES

Ref.	Type and Description	Code No.
Q108/109/110 Q111/112/113 Q114/115 Q120/121/122 Q124/125 Q116/117 Q118/123 Q126	Transistor General Purpose NPN (Typical BC.547) Transistor General Purpose PNP (Typical BC557)	19-5780-5 19-5782-1
D100/101	Diode IN4148	19-3992-0

XTALS/INDUCTORS/TRIMMERS

Ref.	Type and Description	Code No.
X100	Crystal - 4.43361875 MHz	16-1898-9
L100	Choke - 10uH Axial	15-7528-7
L101	Coil - Chrominance Rejector	85-9640-9
C131	Trimmer - Capacitor 3-40 pf	14-6692-5

CONNECTORS

Ref.	Type and Description	Code No.
M100/101	Conn.8-way plug 22-03-2081 Molex	22-7627-5
	Conn.2-way shunt 15-38-1024 Molex	22-8077-9

MISCELLANEOUS

Ref.	Description	Code No.
U100	U.H.F Modulator UM1286 Astec	21-3623-6

CABINET ASSEMBLY ITEMS

Description	Code No.
Computer - Composite Moulded Base	85-4330-5/20100
Non-Slip Foot	60-5888-4
Computer - Composite Moulded Cover	85-4331-3/20100
Disc Drive - Moulded Blanking Plate	85-4344-5/20100
Moulded Knob	85-4348-8
Keyboard and Speaker Assembly	05-2081-0
Disc Drive Assembly	05-2082-9
Power Supply Unit - Box Retaining Bracket	85-4329-1
Disc Drive Mounting Brackets	85-4342-9
Loudspeaker Assembly	05-2085-5
Power Supply Assembly Complete	05-2005-5
Main P.C.B Computer Assembly Complete	05-2002-0

KEYBOARD AND SPEAKER ASSEMBLY

Description	Code No.
Keyboard Assembly	05-2006-3H
Keyboard - CPU I/Conn. Lead	85/4441-7
Keyboard Cover Moulding	85-4332-1/20100
Loudspeaker 90 x 60mm - 8R Pioneer	21-3625-2
Loudspeaker Wiring Harness	05-2085-3
L.E.D. Display Assembly	05-2079-9
Speaker Grill Moulding	85-4340-2/20110
Moulded Window - Key Functions Indicator	85-4343-7

DISC DRIVE ASSEMBLY (SINGLE DRIVE UNIT)

COMPONENT PARTS DESCRIPTION	Code No.
Wiring Harness - Disc Drive Power Lead Set	05-2086-1
Wiring Harness - Disc Drive Control Lead Set	05-2083-7
Disc Drive - 3" FD30A TEAC.	17-0001-4
Disc Drive - Screening Case	85-4349-6/A
Disc Drive - Mounting Screw - M3 x 6mm Pan.hd	40-0366-7

SWITCH MODE POWER SUPPLY

RESISTORS (EXCEPT 0.25W 5% CARBON FILM)

Ref.	Value	Tol.%	Wattage	Type/Description	Code No.
RE01	3R3	10	3	Wire Wound	11-5105-3
RE02	12k	5	7	Wire Wound	11-5078-7
RE05	390k	5	0.5	C. Film	11-3575-9
RE08	150k	5	0.5	C. Film	11-2668-7
RE10	120k	5	0.5	C. Film	11-2688-7
RE15	15k	5	7	Wire Wound	11-4858-7
RE16	100R	5	1	C. Film	11-4999-7
RE17	10R	10	0.7	Metal Film Fusible	11-4294-1
RE18	3M3	5	0.5	Metal Glaze - Mullard	11-4294-1 ⚠
RE24	2K2	20	-	Preset - Min Carbon	12-2467-0
RE02/M					
RE05/M	-	-	-	Resistor Mounting Brkt	25-1493-1

Switch Mode Power Supply (Contd.)

CAPACITORS

Ref	Value	Tol.%	Voltage	Type	Code No.
CE01	220n	20	250.AC	--	14-5163-4 ⚠
CE02	100u	-10+20	385	E	14-6666-6
CE03/05/18	100u	-20+50	25	E	14-3657-0
CE04	220u	-20+50	16	E	14-5745-4
CE06	33P	5	50	CA	14-6604-6
CE07	2n2	20	50	CA	14-6358-6
CE08	10n	5	400	MP	14-6805-7
CE10	150n	10	250	MP	14-4387-9
CE11/20	100n	20	250	MP	14-4386-0
CE12	1n5	5	1.5Kv	MPP	14-6649-6
CE13	10n	20	250	MP	14-4380-1
CE14	47n	20	400	MP	14-4419-0
CE15	1n8	-20+40	250.AC		14-6865-0 ⚠
CE16	2200u	20	16	E	14-6828-6
CE17/21					
CE22	1000u	20	16	E	14-6827-8
CE23	22u	-20+50	16	E	14-2821-7
CE24	10u	-20+50	16	E	14-3620-1

INTEGRATED CIRCUITS

Ref.	Type and Description	Code No.
IE01	TDA 4600-2D Siemens	19-8118-8
IE02	LM79 L12 ACZ Nat.Semi.	19-8081-5

TRANSISTORS ETC.,

Ref.	Type and Description	Code No.
QE01	BU462A	
QE02/03	Gen. Purpose Trans. (Eg. Typical BC547)	19-5780-5
KE01	4N27 Opto Isolator	19-8027-0 ⚠

DIODES

Ref.	Type and Description	Code No.
DE01/02		
DE03/04	BY127 Diode	19-4636-6
DE05/10	BA159 Diode	19-7779-2
DE06/07		
DE08/12	BA157 Diode	19-4028-7
DE11	BY396 Diode	18-2222-5
DE13	BYU 19.35 Diode Mullard	19-8082-3
DE14	TIC126 - Thyristor	19-7610-9
DE15/16	BZX79 - C5V1 5% 350mv Volt.reg.	19-6295-7

Switch Mode Power supply (contd.)

TRANSFORMERS/CHOKES/INDUCTORS ETC.,

Ref.	Description	Code No.
TEQ1	Transformer - SM PSU Computer	85-9629-8 ⚠
ZE01	Mains Filter Choke. 682723-62B8 Siemens	15-7344-6 ⚠
LE01	Ferrite Bead FX401 Mullard	15-7612-7
LE02	Choke - 3u3H	85-3833-6
LE03/04	Choke - 4u7H	85-9633-6

MISCELLANEOUS

Ref.	Description	Code No.
-	Mains On/Off Rocker Switch 2600-11E Arrow Hart	20-4056-5 ⚠
-	Mains Lead Assembly (3 Core)	05-2007-1 ⚠
FE01	Fuse 1A Time Lag	21-3308-3 ⚠
-	Wiring Harness - Power Supply	05-2010-1
-	Strain Relief Bush - R5 Richo	23-4332-0
-	P.S.U Box Base Pressing	85-4328-3
-	P.S.U Box Cover Pressing	85-4327-5

LIST OF ASSEMBLIES USED IN COMPUTER TC01 - EINSTEIN

Description	Code No.
Switched Mode Power Supply Unit Comprising:-	05-2005-5
Main PCB Power Supply	05-2005-5H
Heatsink Switch Mode Transistor Assembly	05-1056-4
Heatsink Regulator/Thyristor Assembly	05-2009-8
Wiring Harness Power Supply	05-2010-1
Mains Lead Assembly	05-2007-1
Mains Connector PSU Leads	05-2012-2
Main PCB Computer Assembly	05-2002-0
Keyboard and Speaker Assembly Comprising:-	05-2081-5
Keyboard Assembly	05-2006-8
Speaker Assembly	05-2084-3
Wiring Harness - Speaker Assembly	05-2085-1
Wiring Harness - LED Display Assembly	05-2082-2
PCB. LED Display	05-2079-9
Disc Drive Assembly	05-2082-9
Wiring Harness - Disc Drive Control - Lead Set (Single)	05-2083-7
Wiring Harness - Disc Drive Power - Lead Set	05-2086-1

APPENDIX A

DISPLAY MONITOR SIGNAL OPTIONS

Facilities are available on the EINSTEIN home computer for feeding the display monitor, with either Y.U.V. - or, with R.G.B output signals.

Selection of the desired standard, is determined by the positioning of 4 'Mini-Shunt' links located on the main printed circuit board assembly.

Normally as supplied, the computer is set to provide Y.U.V. signals, via the Din 6-pin 'Video' output socket, located on the rear of the computer housing, and marked - YUV-RGB LINEAR (INT.SELECT).

To change to R.G.B. format - proceed as follows:-

* As described previously in Section 2.2, 'Construction and Service Access'; unplug the mains lead and other external interconnecting cables and carefully remove the moulded top cover.

* With the cover removed, refer to Figs. 1A & Fig 2A. These diagrams show respectively, the operation of changing the positions of the links themselves and the locations of the 'Mini-Shunt' plug link connectors (M100 and M101) on the main P.C.B. Link positions for Y.U.V. format, are shown in chain dotted outline.

Positions for the change to R.G.B. format, are shown in solid outline.

Take care to unplug <u>all 4 links</u> and replace them into the new positions indicated.

* Finally, replace the top cover-ensuring it is correctly seated before refitting the 2 retaining screws.

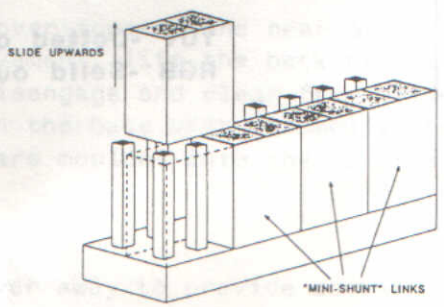


FIG.1A CHANGING OPERATION - 'MINI-SHUNT' LINK CONNECTIONS

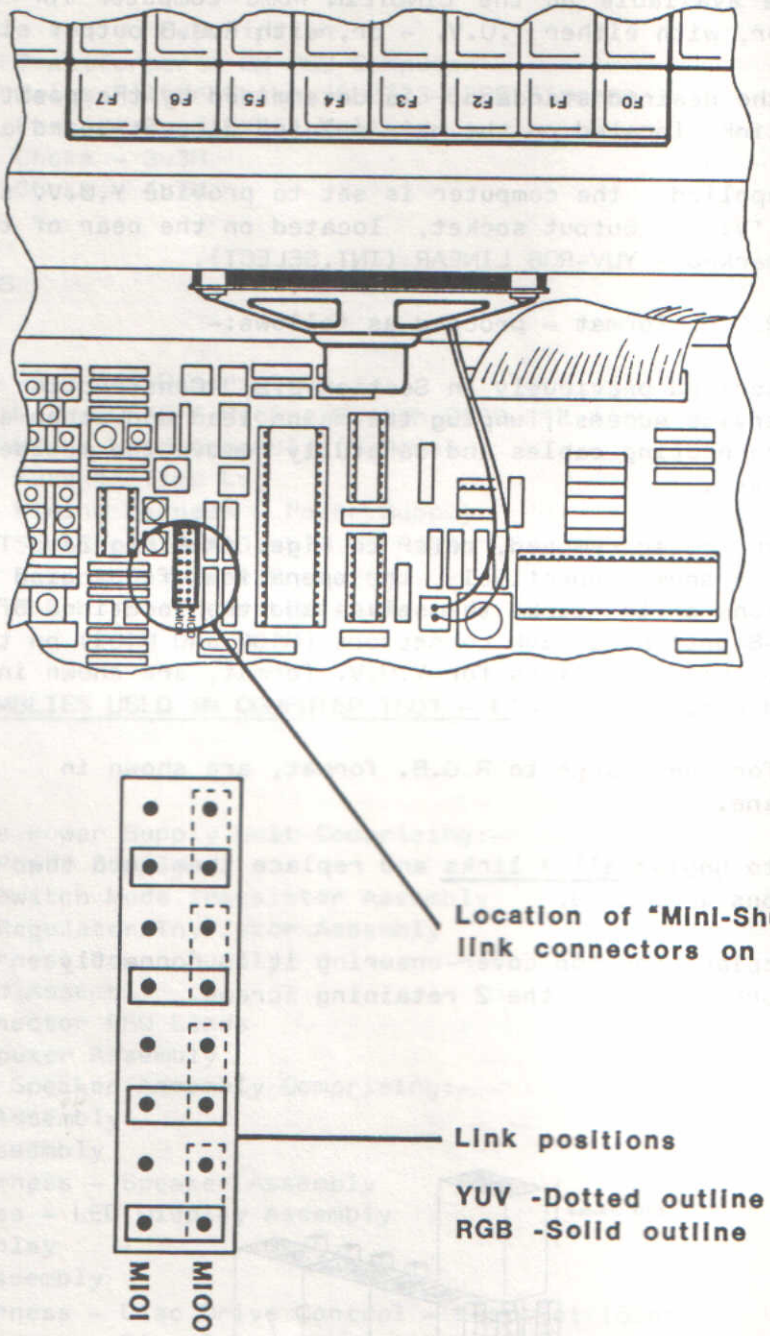


Fig. 2A. DISPLAY MONITOR - SIGNAL OPTIONS

APPENDIX B

INSTALLING A SECOND DISC DRIVE UNIT

A second disc drive unit may be installed into the location provided and marked DRIVE 1/B on the front fascia of the EINSTEIN Home Computer.

Normally, this second disc drive is supplied as an optional extra for installation by the user, or by the dealer.

When supplied as a kit, the contents comprise:-

1 x Disc Drive Unit - Part No. 17-0001-4

1 x Disc Drive Screening Can - Part No. 85-4349-6/A

4 x Disc Drive mounting screws (Pozi-Panhead M3 x 6mm) - Part No 40-0366-7

1 x Internal Dual Disc Drive Control Harness Lead Set with double multiway ribbon connectors. (M005A) Part No. 85-2325-9

1 x Disc Drive Power Harness Lead Set (M009) Part No. 05-2086-1

To install the second disc drive unit:-

First, switch-off the power supply, unplug the mains lead from the mains power supply and disconnect all other external interconnecting cables.

Access:
To gain access for installation of the disc drive:-

* Unscrew and remove the 2 retaining screws located in the rear face of the computer's top cover.

* Slide the cover towards the rear of the unit - and, in the same movement, lift the back of the cover gently. This will disengage and clear from their respective locations in the base unit assembly, the 4 retaining lugs which are moulded into the cover's front top and sides.

* Lift the cover away to provide access.

Preparation:
To prepare for the second drive unit:

* Remove the single screw retaining the DRIVE 1/B aperture blanking plate, from inside the fascia/ speaker baffle moulding and detach the plate. Refit the retaining screw into the fascia/ speaker baffle moulding.

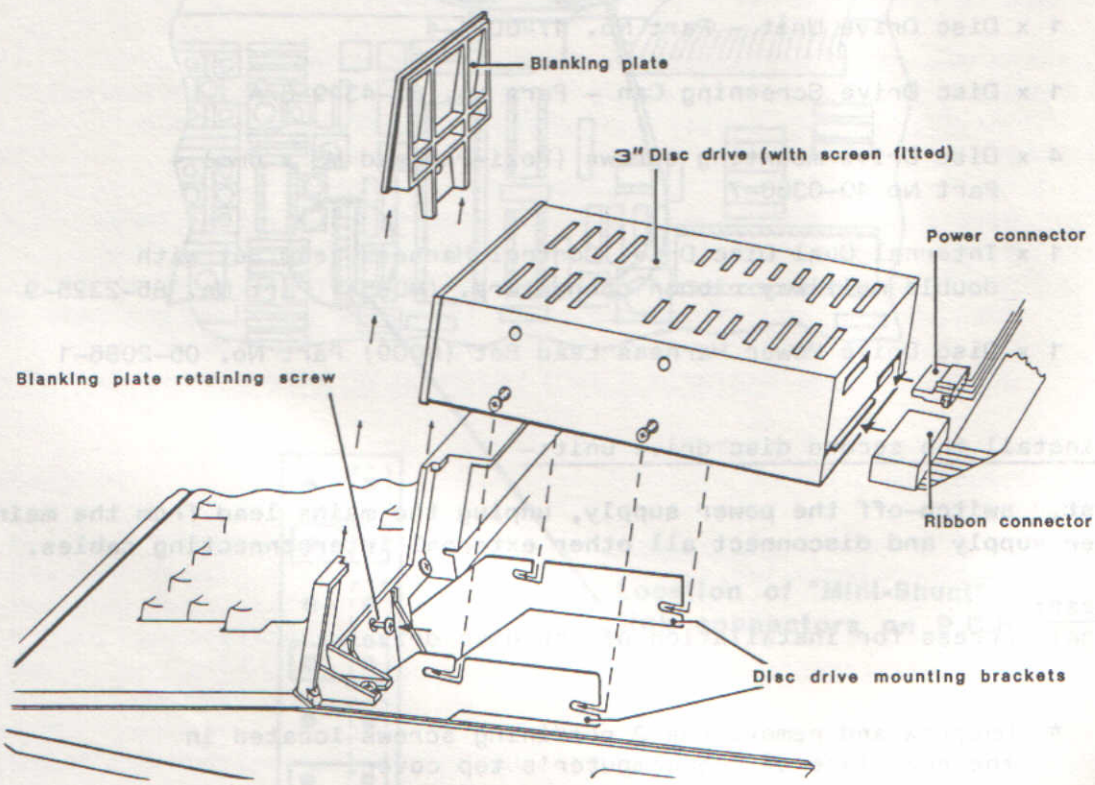


Fig.1. INSTALLING A SECOND DISC DRIVE

* Unplug the existing multiway ribbon connector on the control harness, from connection M005 on the main P.C.B. Unplug the other end of this lead from the back of the existing disc drive unit.

* Unscrew the 2 screws retaining the speaker unit to the speaker baffle moulding - unplug the speaker connection on the main P.C.B. (M011) and temporarily remove the speaker, taking care not to damage the speaker cone.

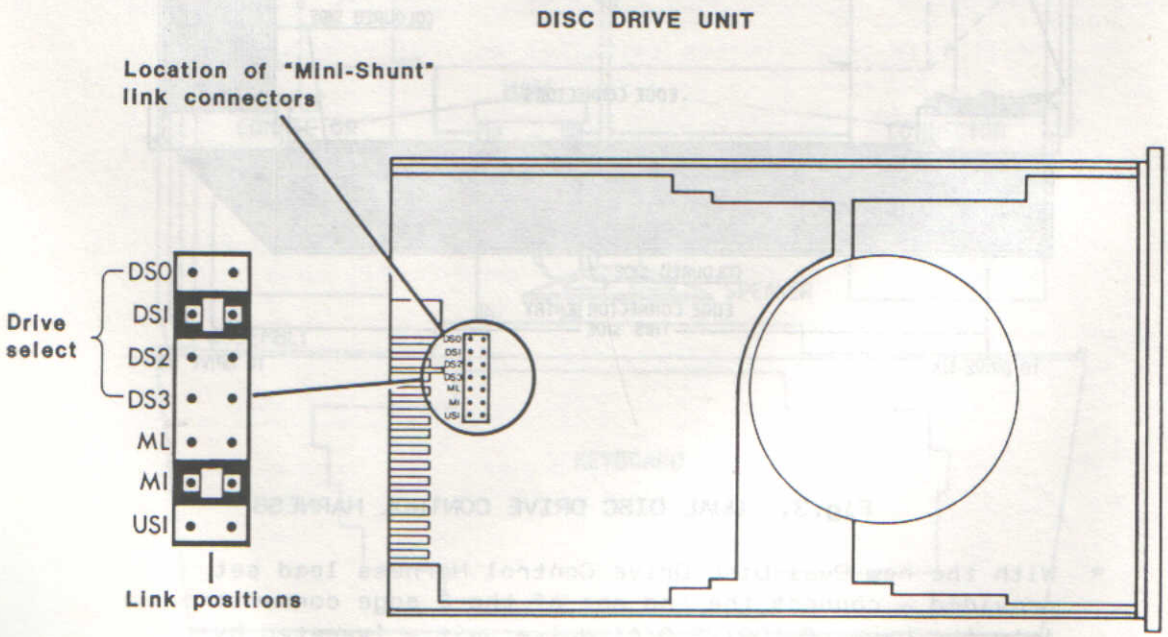
Drive Unit:

IMPORTANT:

* Before fitting the screening can to the new drive unit, the unit will require programming for correction functioning.

  This is done by adjustments of miniature link connectors (MINI-SHUNTS) - the positions of which should be as shown in the diagram Fig. 2. To effect the change, the individual links must be unplugged and repositioned as shown.

* Fit the drive unit into its screening can, ensuring that the apertures in the back, are correctly aligned with the connectors on the drive unit's printed circuit board. Screw in - but not fully at this stage - the 4 threaded retaining screws (m3 x 6mm), into the holes provided at the sides of the screening can and drive unit.



Installation- 2nd. Disc drive unit- Link connector details showing drive select link in second (internal) drive position

Fig.2. LINK CONNECTION ADJUSTMENTS

Installation:
To install the second drive unit:

Lead Sets:

* Prior to installing the Dual Disc Drive Control Harness lead set, the ribbon cable forming the lead set may be dressed and folded as shown in Fig 3 to provide a neat installation.

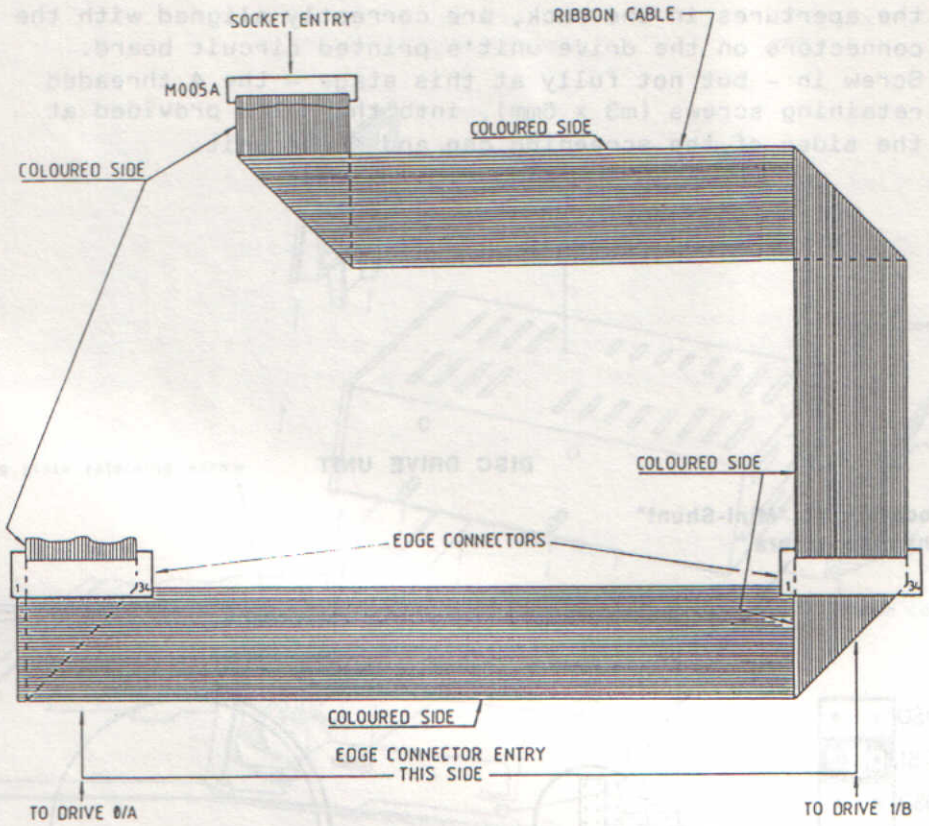
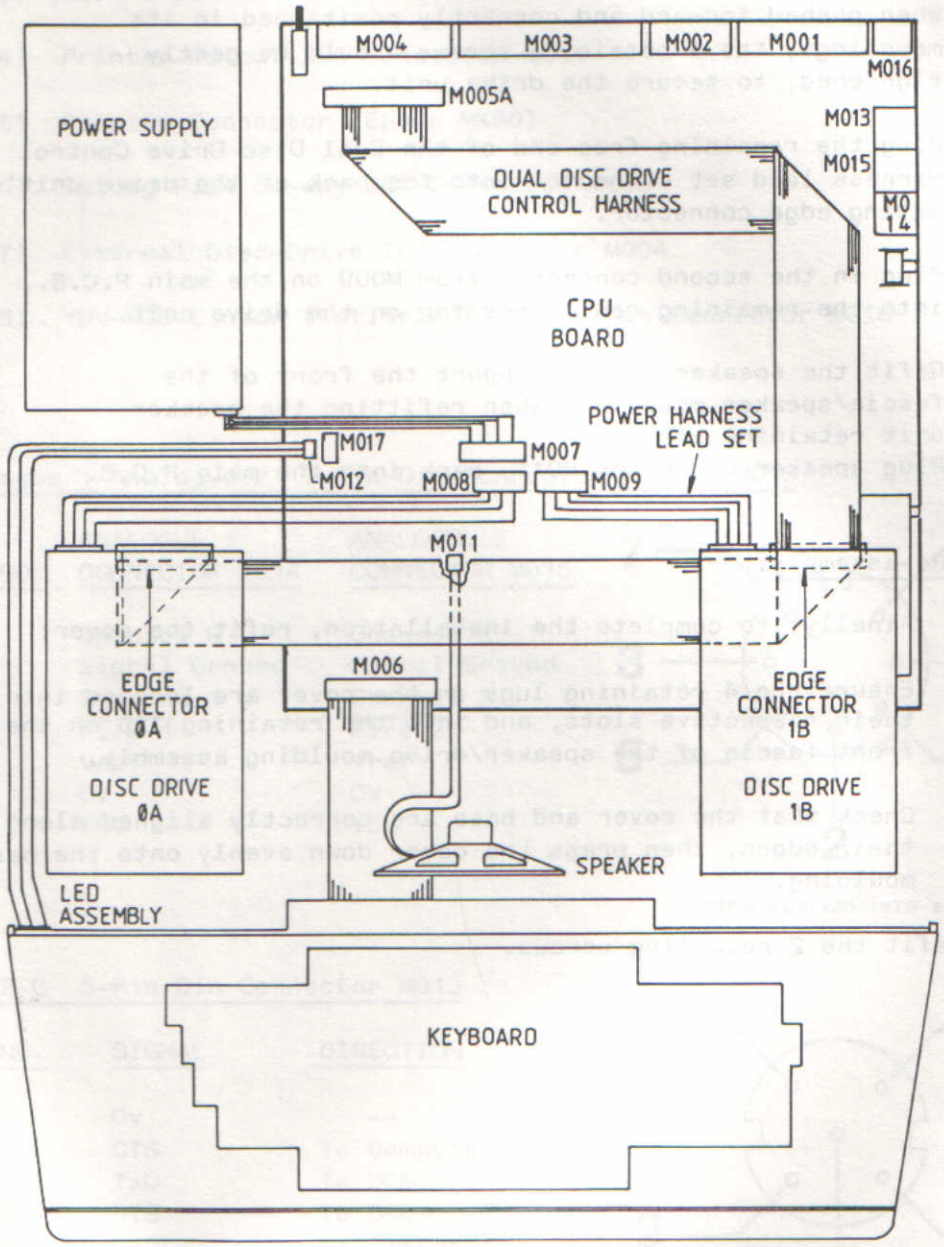


Fig.3. DUAL DISC DRIVE CONTROL HARNESS

* With the new Dual Disc Drive Control Harness lead set provided - connect the end one of the 2 edge connectors into the back of 'DRIVE 0/A' drive unit - (vacated by the original lead set previously removed).

  Connect the opposite end of the lead set, into connector M005 on the main P.C.B. Dress and position the ribbon lead in the manner and direction, Shown in Fig 4.

  The remaining central lead edge connector is then available, ready to install into the new disc drive unit at location DRIVE 1/B



DRAWING NUMBER 85-4359-3

Fig.4. DUAL DISC DRIVE INTERCONNECTION DIAGRAM

Lead Set: (Contd)

* Plug the Power Harness lead set provided, into the mating connection M009 on the main P.C.B.

  The front of the drive unit should be offered into the aperture in the fascia and the shanks of the mounting screws engaged into the slots in the drive unit mounting brackets.

  When pushed forward and correctly positioned in its mountings, the 4 retaining screws should be gently tightened, to secure the drive unit.

* Plug the remaining free end of the Dual Disc Drive Control Harness lead set connector into the back of the drive unit's mating edge connector.

* Plug in the second connector from M009 on the main P.C.B., into the remaining rear connector on the drive unit.

* Refit the speaker unit - support the front of the fascia/speaker moulding, when refitting the speaker unit retaining screws.
  Plug speaker connector M011, back into the main P.C.B.

Cover Re-assembly:

* Finally, to complete the installation, refit the cover:

  Ensure the 4 retaining lugs on the cover are located into their respective slots, and into the retaining lip on the front fascia of the speaker/drive moulding assembly.

  Check that the cover and base are correctly aligned along all their edges, then press the cover down evenly onto the base moulding.

Refit the 2 retaining screws.

APPENDIX C

EXTERNAL SOCKETS AND CONNECTORS - Pin Specifications

1) Analogue 1/Analogue 2 7-Pin Din Connectors M014 & M015

2) RS232-C 5-Pin Din Connectors M013

3) User Input/output IDC Connector M002

4) Printer Output IDC Connector M001

5) Printer Connector (Epson MX80)

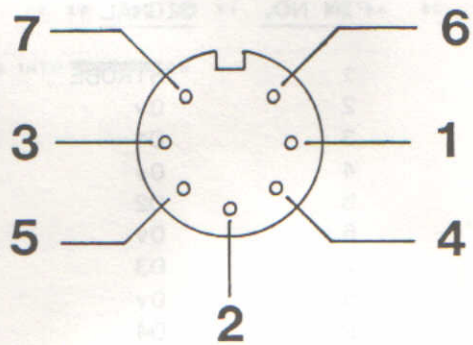
6) Tatung Pipe 60-way IDC Connector M003

7) External Disc-Drive IDC Connector M004

8) YUV-RGB Linear (Int.Select) 6-Pin Din Connector M016

1) Analogue 1/Analogue 2 7-Pin Din Connector M014 & M015

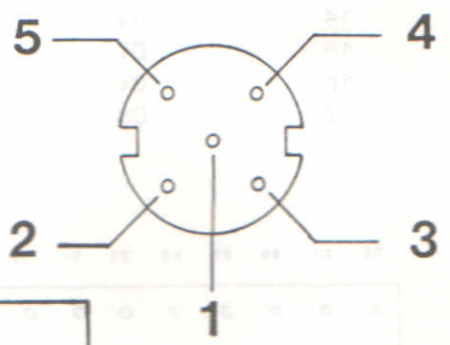
PIN NO.	ANALOGUE 1 CONNECTOR M014	ANALOGUE 2 CONNECTOR M015
1	Channel 0	Channel 2
2	Signal Ground	Signal Ground
3	Channel 1	Channel 3
4	Fire 1	Fire 2
5	Vref	Vref
6	OV	OV
7	+5V	+5V



VIEW LOOKING INTO SOCKET

2) RS232-C 5-Pin Din Connector M013

PIN NO.	SIGNAL	DIRECTION
1	Ov	--
2	CTS	To Computer
3	TxD	To DCE
4	RTS	To DCE
5	RxD	To Computer

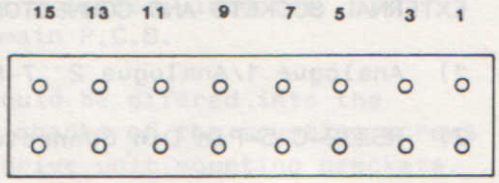


VIEW LOOKING INTO SOCKET

Key:-
DCE - Data Communication equipment (e.g. MODEM)
TxD - Transmit Data
RxD - Receiver Data
CTS - Clear to Send
RTS - Request to Send

3) User Input/output IDC Connector M002

PIN NO.	SIGNAL
1	5V
2	D0
3	0v
4	D1
5	RDY
6	D2
7	0v
8	D3
9	0v
10	D4
11	$\overline{\text{STB}}$
12	D5
13	0v
14	D6
15	5v
16	D7

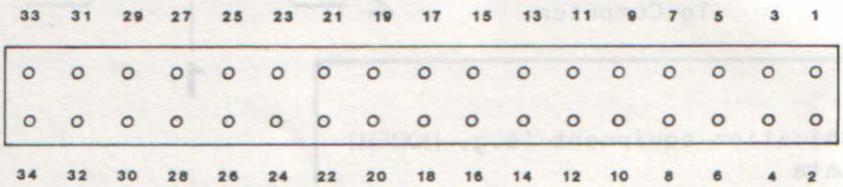


VIEW LOOKING INTO CONNECTOR

Key:-
D - Data Bit
ACK - Acknowledge
PE - Paper End
N/C - No Connection

4) Printer Output IDC Connector M001

PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	$\overline{\text{STROBE}}$	18	0v
2	0v	19	$\overline{\text{ACK}}$
3	D1	20	0v
4	0v	21	BUSY
5	D2	22	0v
6	0v	23	PE
7	D3	24	0v
8	0v	25	N/C
9	D4	26	N/C
10	0v	27	N/C
11	D5	28	$\overline{\text{ERROR}}$
12	0v	29	N/C
13	D6	30	NC
14	0v	31	0v
15	D7	32	N/C
16	0v	33	0v
17	D8	34	N/C

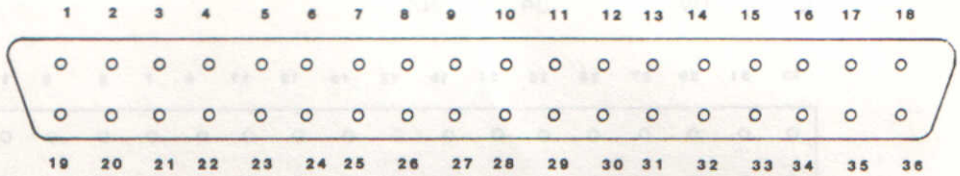


VIEW LOOKING INTO CONNECTOR

5) Printer Connector (Epson MX80)

PIN NO.	SIGNAL	RETURN
1	$\overline{\text{STROBE}}$	Pin 19
2	D1	20
3	D2	21
4	D3	22
5	D4	23
6	D5	24
7	D6	25
8	D7	26
9	D8	27
10	$\overline{\text{ACK}}$	28
11	BUSY	29
12	PE	30
13	N/U	
14	N/U	
15	N/U	
16	0v	
17	GND	
18	N/C	
31	N/U	
32	$\overline{\text{ERROR}}$	
33	N/U	
34	N/C	
35	N/U	
36	N/C	

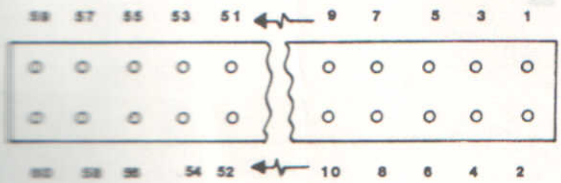
KEY:-
D - Data Bit
N/U - Not used by the TATUNG COMPUTER
N/C - No Connection
ACK - Acknowledge
PE - PAPER END



VIEW LOOKING INTO CONNECTOR

6) Tatung 'Pipe' Connector - PL3 - 60 way IDC

PIN NO.	SIGNAL	PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	+5V	21	A12	41	0v
2	D7	22	A11	42	$\overline{\text{WR}}$
3	+5V	23	A10	43	0v
4	D6	24	A9	44	$\overline{\text{RD}}$
5	0v	25	A8	45	0v
6	D5	26	A7	46	$\overline{\text{IORQ}}$
7	0v	27	A6	47	0v
8	D4	28	A5	48	$\overline{\text{MREQ}}$
9	0v	29	A4	49	0v
10	D3	30	A3	50	$\overline{\text{HALT}}$
11	0v	31	A2	51	0v
12	D2	32	A1	52	$\overline{\text{NMI}}$
13	0v	33	A0	53	0v
14	D1	34	$\overline{\text{RST}}$	54	$\overline{\text{INT}}$
15	0v	35	0v	55	0v
16	D0	36	$\overline{\text{RFSH}}$	56	$\overline{\text{WAIT}}$
17	0v	37	0v	57	0v
18	A15	38	$\overline{\text{M1}}$	58	$\overline{\text{BUSREQ}}$
19	A14	39	0v	59	0v
20	A13	40	$\overline{\text{BUSACK}}$	60	SYS CLK (4MHz)



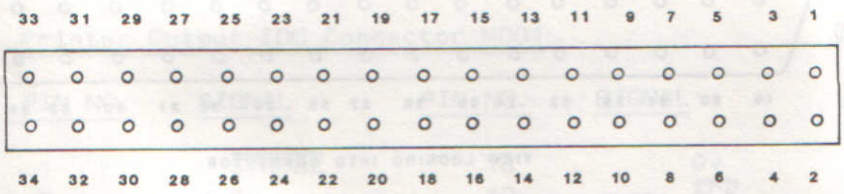
ARROW ON TOP OF CONNECTOR INDICATES PIN-1

7) External Disc Drive IDC Connector M004

PIN NO.	SIGNAL	PIN NO.	SIGNAL	DIRECTION
1	0v	2	N/C	---
3	0v	4	N/C	---
5	0v	6	D/S-3	TO DRIVE
7	0v	8	INDEX	TO COMPUTER
9	0v	10	D/S-0	TO DRIVE
11	0v	12	D/S-1	TO DRIVE
13	0v	14	D/S-2	TO DRIVE
15	0v	16	MOTOR ON	TO DRIVE
17	0v	18	DIR/S	TO DRIVE
19	0v	20	STEP	TO DRIVE
21	0v	22	WRITE DATA	TO DRIVE
23	0v	24	WRITE GATE	TO DRIVE
25	0v	26	TRACK 0	TO COMPUTER
27	0v	28	WRITE PROTECT	TO COMPUTER
29	0v	30	READ DATA	TO COMPUTER
31	0v	32	SIDE-SELECT	TO DRIVE
33	0v	34	N/C	

KEY:-

N/C - No connection
D/S - Drive-Select
DIR/S - Direction Select



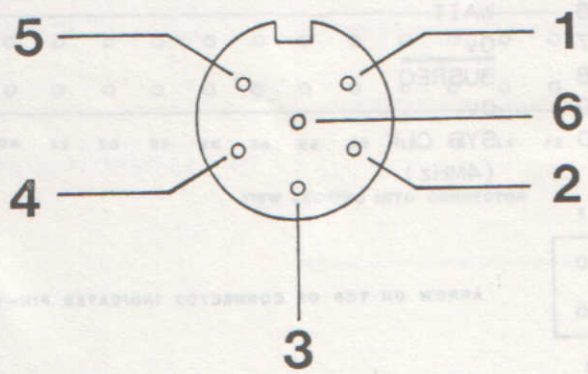
VIEW LOOKING INTO CONNECTOR

8) YUV-RGB Linear (Int. Select), 6-Pin Din Socket for Video

PIN NO.	RGB OUTPUT *	YUV OUTPUT *
1	R	V
2	G	Y+syncs
3	B	U
4	Syncs	0v
5	0v	0v
6	N/C	N/C

N/C = No Connection

* The outputs are internally user selectable via link switches M100 and M101. (See APPENDIX A)



VIEW LOOKING INTO SOCKET